DC capacitor-less inverter for single-phase power conversion with minimum voltage and current stress

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Abstract—Single-phase power conversion such as PWM rectifier, grid connected PV inverter system, static synchronous compensator (STATCOM) all can be implemented by an H-bridge inverter and a large electrolytic dc capacitor to absorb the ripple power pulsating at twice the line frequency (2ω ripple power). This paper proposed a dc capacitor-less inverter for H-bridge with minimum voltage and current stress. By adding another phase leg to control an ac capacitor, the 2ω ripple power can be absorbed by the capacitor and theoretically 2ω ripples to the dc capacitor can be eliminated completely. The H-bridge and the addition phase leg can be analyzed together as an unbalanced three phase system. By adopting SVPWM control and choosing the optimum ac capacitance and the voltage reference, the voltage and current stress of the switches can be minimized to the same as the conventional H-bridge. The size of capacitor is reduced by 10 times compared to the conventional H-bridge system. Simulation and experimental results are shown to prove the effectiveness of the proposed dc capacitor-less inverter and active power decoupling method.

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Index Terms— dc capacitor-less inverter, single-phase power conversion, H-bridge, 2ω ripple, power decoupling, SVPWM, current and voltage stress.

I. INTRODUCTION

H-bridge has been widely used for single-phase power conversions, such as PWM rectifier, grid connected PV inverter and static synchronous compensator (STATCOM) [1-5]. Although the power factor (PF) for these applications could be different, however, they have a common inherent problem of instantaneous power unbalance between dc power and ac power, which is time varying with a double-frequency variation. In order to absorb the 2ω ripple power, conventional H-bridge needs a bulky and expensive dc capacitor. The dc capacitance is given by

$$C = \frac{S}{2\pi f V_{dc} \Delta V_{dc}}.$$  \hfill (1)

where \(f\) is line frequency, \(S\) is the rated apparent power of the system, \(V_{dc}\) is the average voltage across the dc capacitor, \(\Delta V_{dc}\) is the allowed peak-to-peak voltage ripple.

In order to reduce the dc capacitor bank, a great deal of research has been done on active power decoupling methods [6-21]. The basic idea is using extra energy-storage components such as capacitor or inductor, which permits much larger fluctuation of the voltage or current, to balance the 2ω ripple power. Therefore, both the energy-storage component and the dc capacitor for switching ripple can be minimized in size and weight. The key point is how to minimize the energy-storage component, number of extra switches, and voltage/current stress of both switches and passive components.

In Fig. 1 (a), the energy-storage capacitor is connected to dc link and the capacitor voltage can only be unipolar [9-11]. If the capacitor voltage reference is a full-wave rectified sine wave, the 2ω ripple power can be fully transferred to the capacitor. However, the full-wave rectified sine reference, which contains rich harmonic content, is difficult for the control system to track. Although it is possible to
lower the harmonic content in the reference by increasing the energy-storage margin (therefore the voltage does not go down to zero), this will compromise full utilization of the energy-storage capacitor.

![Diagram](image)

(a)

![Diagram](image)

(b)

![Diagram](image)

(c)

Fig. 1 H-bridge with active power decoupling topologies

A single-phase PWM rectifier with the power decoupling ripple-port shown in Fig. 1 (b) is proposed in [12]. By adding any extra H-bridge to interface the energy-storage capacitor, the capacitor works in ac mode and the voltage/current waveforms are sinusoidal. Since the energy-storage capacitor is fully utilized, the capacitance is minimized. However, the system needs too many auxiliary switches, which
increases the system complexity.

In [13-14], the PWM rectifier system shown in Fig.1 (c) consists of an H-bridge and an additional phase leg connected to an AC capacitor, $C_{ac}$. Compared to the topology in Fig.1 (b), the number of extra switches is reduced. However, because of the adoption of SPWM control, the dc voltage is greatly increased. As a result, the voltage stress of switches is higher; size and weight of passive components are larger.

In this paper, the proposed dc capacitor-less inverter for single-phase power conversion has the same topology in Fig.1(c). However the system is analyzed as an unbalance three-phase system. By adopting SVPWM control and choosing the optimum ac capacitance and the voltage reference, the topologies can be used for PWM rectifier (PF = 1), inverter (PF = −1) and STATCOM (PF = 0, current leading voltage) without increasing both current and voltage stress. Since only two more switches are needed and voltage/current stress is the same as the original H-bridge, the total device power rating is only increased by 50%. The total size of capacitor (including the ac capacitor and the dc capacitor) of the proposed system is reduced by 10 times compared to conventional H-bridge system.

II. THEORETICAL ANALYSIS

Taking the three output voltages of the three phase-legs as controlled voltage sources $v_a$, $v_b$, $v_c$, the equivalent circuit for Fig.1 is shown in Fig. 2.

A. Power flow analysis

Suppose the grid voltage and the rated grid-side current to be:

\[
\begin{align*}
  v_s &= V_s \sin(\omega t) \\
  i_s &= I_s \sin(\omega t + \varphi)
\end{align*}
\]

and the voltage and current of the storage ac capacitor to be:
\[ v_{\text{Cac}} = V_{\text{Cac}} \sin(\omega t + \vartheta) \]
\[ i_{\text{Cac}} = I_{\text{Cac}} \cos(\omega t + \vartheta) = \omega C_{\text{ac}} V_{\text{Cac}} \cos(\omega t + \vartheta) \]

(3)

Then, we can get the expression of grid power:

\[ p_x = v_x i_x = \frac{1}{2} V_s I_s [\cos(\varphi) - \cos(2\omega t + \varphi)] = \frac{1}{2} V_s I_s [\cos(\varphi) + \sin(2\omega t + \varphi - \frac{\pi}{2})] \]

(4)

and the \( 2\omega \) ripple power part of \( p_x \) is

\[ p_{2\omega} = \frac{1}{2} V_s I_s \sin(2\omega t + \varphi - \frac{\pi}{2}) \]

(5)

The instantaneous power generated by \( C_{\text{ac}} \) can also be obtained:

\[ p_{\text{Cac}} = v_{\text{Cac}} i_{\text{Cac}} = \frac{1}{2} \omega C_{\text{ac}} V_{\text{Cac}}^2 \sin(2\omega t + 2\vartheta) \]

(6)

To simplify the analysis, the power on filter inductors \( L_{f1} \) and \( L_{f2} \) (which are normally less than 5% pu) is neglected. Then, the power of \( C_{\text{ac}} \) should be controlled equal to the grid \( 2\omega \) ripple power:

\[ p_{\text{Cac}} = p_{2\omega} \]

(7)

Therefore, the magnitude and phase of \( v_{\text{Cac}} \) should satisfy the following equations:

\[ \omega C_{\text{ac}} V_{\text{Cac}}^2 = V_s I_s \]
\[ \vartheta = \frac{1}{2}(\varphi - \frac{\pi}{2}), \text{ or } \frac{1}{2}(\varphi - \frac{\pi}{2}) + \pi \]

(8)

If the decoupling capacitance is designed to be

\[ C_{\text{ac}} = \frac{I_s}{\omega N_s} \]

(9)

the magnitude of the voltage and current of \( C_{\text{ac}} \) will be:
\[ V_{ac} = V_s, \quad I_{ac} = I_s, \quad (10) \]

and the current and voltage stress of the system can be minimized.

**B. Specific cases analysis**

According to the previous analysis, for any φ, there are two possible solutions of θ. Because the system can be treated as an unbalanced three phase system, SVPWM can be adopted. For SVPWM, the minimum dc voltage is determined by the maximum line-to-line voltage. For the rated power, we have:

\[ \left| \vec{V}_{ab} \right| = \left| \vec{V}_{cb} \right| = \left| \vec{V}_{ac} \right|, \quad \left| \vec{I}_a \right| = \left| \vec{I}_c \right| = \left| \vec{I}_{ac} \right|, \quad (11) \]

For PWM rectifier, inverter and STATCOM, there will be two possible solutions for θ. Only by choosing θ to be \(-\frac{\pi}{4}, \frac{\pi}{4}\) and 0 for PWM rectifier, inverter and STATCOM respectively, the magnitude of \( \vec{V}_{ac} \) is smaller than \( V_s \), and the magnitude of \( \vec{I}_b \) is smaller than \( I_s \). Then, the voltage stress is \( \sqrt{2}V_s \), and the current stress is \( \sqrt{2}I_s \). Therefore, the voltage and current stress of switches are equal to the original H-bridge system. If θ is not chosen properly, the current and voltage stress will be greatly increased. For example, θ can also be \( \pi \) for STATCOM case. However, the magnitude of \( \vec{V}_{ac} \) will be \( 2V_s \), and the magnitude of \( \vec{I}_b \) will be \( 2I_s \), and the voltage and current stress will be doubled. Fig.3 shows the phasor diagrams of three specific cases with the minimum voltage and current stress.

Because the voltage and current stress of the proposed system and the H-bridge system are the same, the two systems can use the same rating switches, and the power loss on switch can be directly compared based on the phase current. For full rated power, phase A and phase C’s leg current of the proposed circuit are same as the two leg of conventional H-bridge system, and phase B’s current of proposed circuit are always smaller than H-bridge’s phase current. Then, the power loss on phase A and C together are almost equal to the H-bridge system; and the power loss on phase B is always
smaller than half of the H-bridge system. Therefore the total switch power loss of the proposed circuit is less than 150% of the H-bridge system.

![Phasor diagram of PWM rectifier, Inverter and STATCOM](image)

(a) PWM rectifier (PF = 1), $\phi = 0$, $\theta = -\frac{\pi}{4}$

(b) Inverter (PF = -1), $\phi = \pi$, $\theta = \frac{\pi}{4}$

(c) STATCOM (PF = 0), $\phi = \frac{\pi}{2}$, $\theta = 0$

Fig.3 Phasor diagrams of PWM rectifier, Inverter and STATCOM

C. General case analysis

Fig.4 shows the phasor diagram of general case. The angle between $\dot{V}_{ab}$ and $\dot{V}_{ac}$ is $|\phi|$, and the angle between $\dot{i}_{a}$ and $\dot{i}_{s}$ is $|\phi - \frac{\pi}{2}|$. According to triangle relationship, in order to guarantee that $V_{ac}$ is smaller than $V_{ab}$; and $I_{b}$ is smaller than $I_{s}$, the angle between $\dot{V}_{ab}$ and $\dot{V}_{cb}$, and the angle between $\dot{i}_{a}$ and $\dot{i}_{s}$ should be smaller than $\frac{\pi}{3}$. Then, $\theta$ should satisfy the following equations:
To hold the inequality, the solution of $\theta$ is chosen as:

$$\theta = \frac{1}{2}(\phi - \frac{\pi}{2}),$$  \hspace{1cm} (13)

and accordingly $\phi$ should satisfy:

$$-\frac{\pi}{6} < \phi < \frac{7\pi}{6}.\hspace{1cm} (14)$$

In other words, by choosing the optimum ac capacitance and suitable $\theta$ for $C_{ac}$ voltage reference, the voltage and current stress can be equal to the original H-bridge system when $-\frac{\pi}{6} < \phi < \frac{7\pi}{6}$.

### D. SVPWM control

The $\alpha\beta$ transformation is defined as

$$\begin{bmatrix} v_a \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_s \\ v_b \\ v_{Cac} \end{bmatrix}.$$

Then we can get the trace of the space vector projected on $\alpha\beta$ reference frame based on $v_s$ and $v_{Cac}$. Because line-to-line voltage of the system is unbalanced, the space vector projection on $\alpha\beta$ reference frame is no longer a circle. Instead, the projection becomes be an ellipse or a line.

Fig.5 shows the space vector projections of PWM rectifier, inverter and STATCOM on $\alpha\beta$ reference
frame. The projections of PWM rectifier and inverter become an ellipse; the only difference is the moving direction of the vector: PWM rectifier is clockwise, and inverter is counterclockwise. The projection of STATCOM is a line, the vector moves back and forth along the line.

![Diagram of space vector projections on \( \alpha \beta \) reference frame]

Fig. 5 Space vector projections on \( \alpha \beta \) reference frame

E. Comparison between SVPWM and SPWM

In order to compare the minimum dc voltage requirement for SPWM and SVPWM control, take PWM rectifier case as an example. For SVPWM, the minimum dc voltage is determined by the
maximum peak value of line-to-line voltage. The maximum peak value of line-to-line voltage is 
\[ \sqrt{2}V_{ab}, \quad \sqrt{2}V_{cb} \] which are all equal to \( \sqrt{2}V \). Therefore, the minimum dc voltage is \( \sqrt{2}V \).

For SPWM, \( v_a, v_b, v_c \) are sinusoid voltages. One possible solution is shown in Fig.6 [13] and according to the triangle relationship, we have:

\[
\begin{align*}
V_a &= V_s / 2 \\
V_b &= V_s / 2 \\
V_c &= \sqrt{(V_s / 2)^2 + V_i^2 - \cos 45^\circ V_s^2} = 0.737V_s
\end{align*}
\]

The minimum dc voltage determined by the peak value of \( v_a, v_b, v_c \). Since \( v_i \) has the maximum peak voltage, the minimum dc voltage is \( 2\sqrt{2}V_c \), which is 47% larger than the dc voltage of SVPWM.

![Phase diagram of PWM rectifier for SPWM](image)

**Fig. 6 Phase diagram of PWM rectifier for SPWM**

### III. CONTROL STRATEGY

#### A. \( C_{ac} \) voltage and current reference

In the previous analysis, the filter inductors, \( L_{f1} \) and \( L_{f2} \) are neglected for simplification. In the following analysis, in order to fully absorb the \( 2\omega \) ripple power, the filter inductors are taken into consideration to calculate the voltage and current reference of \( C_{ac} \).

Taking the reactive powers of \( L_{f1} \) and \( L_{f2} \) into account, the instantaneous power of dc capacitor from the grid side becomes:
\[ p_{ab} = v_i i - L_{f1} \frac{di}{dt}, \quad i = \frac{1}{2} V_i I, \cos(\phi) + \]
\[ \frac{1}{2} V_i I, \sin(2\alpha + \phi - \frac{\pi}{2}) - \frac{1}{2} \omega L_{f1} I_1^2 \sin(2\alpha + 2\phi) \] (17)

and the 2\( \omega \) ripple power component is:
\[ p_{ab, 2\omega} = \frac{1}{2} V_i I_1 \sin(2\alpha + \phi - \frac{\pi}{2}) - \frac{1}{2} \omega L_{f1} I_1^2 \sin(2\alpha + 2\phi) \] (18)

where \( P_{ab, 2\omega} = \sqrt{(V_i I_1)^2 + (\omega L_{f1} I_1^2)^2 + 2\omega L_{f1} V_i I_1 \sin \phi} \), and \( \tan \phi_{ab} = \frac{V_i I \cos \phi + \omega L_{f1} I_1^2 \sin(2\phi)}{V_i I \sin \phi - \omega L_{f1} I_1^2 \cos(2\phi)} \).

Similarly, the instantaneous power of dc capacitor from \( C_{ac} \) side becomes
\[ p_{iC_{ac}} = V_{C_{ac}} I_{C_{ac}} = L_{f2} \frac{di_{C_{ac}}}{dt}, \]
\[ V_{C_{ac}} = \frac{1}{2} \frac{V_{C_{ac}}^2}{\omega C_{ac}} \sin(2\alpha + 2\theta) \] (19)

The power from \( C_{ac} \) side should be controlled equal to the 2\( \omega \) ripple power from the grid side:
\[ p_{iC_{ac}} = p_{ab, 2\omega} \] (20)

Therefore, the magnitude and phase of \( V_{C_{ac}} \) should be:
\[ V_{C_{ac}} = \sqrt{P_{ab, 2\omega} \left(\frac{1}{\omega C_{ac}} - \omega L_{f2}\right)} \] (21)
\[ \theta = \frac{1}{2} \phi_{ab} \]

and the magnitude of \( I_{C_{ac}} \) should be:
\[ I_{C_{ac}} = \frac{V_{C_{ac}}}{\omega C_{ac} - \omega L_{f2}} \] (22)

**B. Control diagram**

Fig. 7 shows the control system, which consists of two control loops. The first one is to control the grid current and the second one is to control the voltage and current of the ac capacitor. The sampling frequency is 20 kHz; \( L_{f1} \) and \( L_{f2} \) are 4.5% and 1.5% respectively.
A proportional-resonant (PR) controller is adopted for the grid current control. The transfer function of PR controller is:

\[ G_{pr}(s) = k_p + \frac{2k_r\omega_0 s}{s^2 + 2\omega_0 s + \omega_0^2}. \]  

(23)

The transfer function from \( V_{ab} \) to grid current, \( i \), is

\[ G_{\alpha_{-\text{vab}}}(s) = \frac{1}{L_{fs}s}. \]  

(24)

Taking the delay caused by sampling time, \( T_s \), the grid current loop transfer function is:

\[ G_{\text{g Loop}}(s) = G_{pr}(s) \cdot G_{\alpha_{-\text{vab}}}(s) \cdot \frac{1-e^{-sT_s}}{sT_s}. \]  

(25)

PR controller parameters are as follows: \( k_p=24 \), \( k_r=90 \), \( \omega_0=25 \) and the bode plot is shown in Fig. 8 (a).

PR controller parameters are as follows: \( k_p=8 \), \( k_r=11 \), \( \omega_0=25 \), and the bode plot is shown in Fig. 8 (b).

Accordingly, the transfer function from ac capacitor current reference to ac capacitor current is:

\[ G_{i_{\text{ref}}}(s) = G_{pr}(s) \cdot G_{\alpha_{-\text{vab}}}(s) \cdot \frac{1-e^{-sT_s}}{sT_s}. \]  

(27)

PR controller parameters are as follows: \( k_p=8 \), \( k_r=11 \), \( \omega_0=25 \), and the bode plot is shown in Fig. 8 (b).
\[ G_i(s) = \frac{G_{l_{\text{loop}}}(s)}{G_{l_{\text{loop}}}(s) + 1}. \]  

(28)

For the voltage outer loop, the transfer function from ac capacitor current to ac capacitor voltage is:

\[ G_{v_{\text{oc}}}(s) = \frac{1}{C_w s}. \]  

(29)

The ac capacitor voltage loop transfer function is:

\[ G_{v_{\text{oc}}}(s) = G_{v_{\text{oc}}}(s) \cdot G_i(s) \cdot G_{PR_{\text{oc}}}(s) \cdot \frac{1-e^{-sT}}{sT}. \]  

(30)

PR controller parameters are as follows: \( k_p=1.8 \), \( k_r=5 \), \( \omega_l=25 \), and the bode plot is shown in Fig. 8 (c).

As it shown in the bode plot, by using dual loop control, the ac capacitor control loop can achieve an acceptable bandwidth to track the voltage and current reference.

(a) Grid current loop

(b) Ac capacitor current loop
IV. SIMULATION AND EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed dc capacitor-less inverter and the active power decoupling method, a 1.5-kVA single phase power conversion system is designed. The key parameters are listed below in Table I.

For conventional H-bridge system, if the allowed dc voltage ripple is 2.5%, the dc capacitance is 4.6 mF (15.5 pu). For the proposed single phase power conversion system, because the $2\omega$ ripple power can be absorbed by ac capacitor, theoretically dc capacitor only needs to absorb switching current ripple, of which the capacitance is 100μF (0.33 pu) [22-23]. However, in practice, considering the other frequency ripple power which has not been compensated by ac capacitor, the dc capacitance is designed to be 170 μF (0.55 pu). The ac capacitor calculated based on (8) is 300 μF (1 pu). Compared to conventional H-bridge system, the proposed dc capacitor-less inverter reduces the total size of the capacitor (including dc capacitor and ac capacitor) by 10 times.
The filter inductance $L_{f1}$ is larger than $L_{f2}$ because the system is connected to grid through an isolated transformer, the transformer leakage inductance is also taken into account. For the filter inductance $L_{f2}$, trade-off design is necessary. With smaller $L_{f2}$, the size of passive component can be reduced. One the other hand, with smaller $L_{f2}$, the current switching ripple of $i_{Cac}$ is larger, which may cause higher power losses. Here, $L_{f2}$ is designed to be 0.4 mH (0.015 pu), to make the current ripple within 20%.

![Graph](image)

(a) PWM rectifier (PF = 1)
Fig. 9 shows the simulation results of PWM rectifier, inverter, and STATCOM cases. $v_{a}^{*}$, $v_{b}^{*}$, $v_{c}^{*}$ are the reference signals for controlled voltage sources $v_{a}$, $v_{b}$, $v_{c}$. Because SVPWM is adopted, the reference signals are not sinusoidal, and the dc voltage can be fully utilized. The average value of $v_{dc}$ is
185 V and the ripple voltage is within 3 V (1.5%). The relationship between $v_s$, $v_{Cac}$, $i_s$, and $i_{Cac}$ is consistent with the theoretical analysis.

A 1.5-kVA prototype based on Fig. 1 has been built. Fig. 10 shows the experimental key waveforms of PWM rectifier, inverter and STATCAOM cases. The average dc voltage is 185 V. For all cases, the voltage ripple is within 5 V (2.5%). The reason that the experimental dc voltage ripple is larger than the simulation result is that the grid voltage has harmonics in experiment, which cause high order frequency ripple power. And the ripple power, which has not been compensated by $C_{ac}$, will cause larger voltage ripple on dc capacitor.

Fig. 11 shows the DC ripple FFT analysis of PWM rectifier, inverter and STATCAOM cases. The $2\omega$ (120 Hz) voltage is within 0.5 V, indicating that the proposed dc capacitor-less inverter and active power decoupling method have effectively absorbed the $2\omega$ ripple power.
Fig. 10 Experimental key waveforms
A DC capacitor-less inverter for single-phase power conversion with minimum voltage and current stress is proposed. Only a AC capacitor to absorb $2\omega$ ripple power and a minimum DC capacitor to absorb the switching ripple power are needed. By adopting SVPWM control and choosing the optimum ac capacitance and the voltage reference, the voltage and current stress of the switches can be minimized. The size of the capacitor is reduced by 10 times. Theoretical analysis and experimental results have been presented. The simulation and experimental waveforms are consistent with the theoretical analysis.

REFERENCES


