Survey on Fault-Tolerant Techniques for Power Electronic Converters

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Abstract—With wide-spread application of power electronic converters in high power systems, there has been a growing interest in system reliability analysis and fault-tolerant capabilities. This paper presents a comprehensive review of conventional fault-tolerant techniques regarding power electronic converters in case of power semiconductor device failures. These techniques can be classified into four categories based on the type of hardware redundancy unit: switch-level, leg-level, module-level and system-level. Also, various fault-tolerant methods are assessed according to cost, complexity, performance, etc. The intent of this review is to provide a detailed picture regarding the current landscape of research in power electronic fault-handling mechanisms.

Index Terms—Fault-tolerance, power electronic converters, system reliability, post-fault operation.

I. INTRODUCTION

Power electronic converters—featuring higher efficiency and higher power density—play an increasingly important role in adjustable-speed drives, utility interface of renewable energy resources, flexible high-voltage direct current (HVDC) transmission systems, and electric or hybrid electric vehicles (HEVs) [1]-[3]. However, field experiences have demonstrated that electrolytic capacitors and power switching devices in power electronic converters, such as insulated gate bipolar transistors (IGBTs) and metal-oxide field-effect transistors (MOSFETs), are the most vulnerable components, which challenge the reliability of the system [4]-[5]. Since most of the power electronic converters do not exhibit redundancy, any fault that occurs to components or subsystems will result in interruption of the operation. In certain applications related to personal safety, such as electric drives for vehicles, this unexpected system shutdown will place passengers into areas of potential risks [6].

In critical applications, such as military, financial markets and hospitals, system interruptions could lead to immeasurable economic losses [5], [7]. Therefore, discussion of fault-tolerant power systems and enhanced system reliability attracts much attention among researchers.

References [8]-[9] define some metrics to evaluate power electronic system reliability, such as failure rate, mean time between failures (MTBF), mean time to repair (MTTR), and availability. Since a precise mathematical model is helpful when verifying whether a fault-tolerant design meets expected requirements, empirical-based model and physics-of-failure model are employed while designing components of power electronics systems [10]. With regard to system-level configurations, the markov model is widely adopted [11].

For a fault-tolerant system, the fault diagnosis is the first step once a fault occurs [12]. An accurate and timely detection and protection can prevent fault propagations and catastrophic consequences. The fault-tolerant operation, consisting of fault-isolation and fault-reconfiguration is the next counter-measure, which is always based on hardware redundancy design and corresponding fault-tolerant control. As for fault-tolerant operations, numerous solutions are reported by past literatures. Based on the type of the hardware redundancy, these methods are classified into four categories: 1) switch-level, 2) leg-level, 3) module-level and 4) system-level. For the first solution, various fault-tolerant methods, such as inherently redundant switching states [18]-[32], DC-bus midpoint connection [33]-[57] and redundant parallel or series switches installation [58]-[63], are investigated extensively. In leg-level solutions, the main approach is to add redundant legs in parallel or series connection to main legs [64]-[74]. Among them, the redundant parallel leg solution achieves a better compromise between the system cost and performance, thus becoming a hot area of fault-tolerant research. Cascade multilevel converters (CMCs) and modular multilevel converters (MMCs) are typical topologies with module-level redundancy. Three scenarios including neutral-shift, DC-bus voltage reconfiguration and redundant modules installation are employed [75]-[88]. In industry fields, the parallel redundancy converter approach is widely employed due to higher reliability. Among the above approaches, some system performances during post-fault are degraded. Therefore, these methods can only be applied in fields where a “limp-home” function is allowable after faults. Additionally, it is necessary to explore more practical modified topologies endowed with a full redundant capability.
and therefore can potentially be applied within the industry in the future.

Due to the growing importance and extensive research surrounding the fault tolerance of power converters, the authors feel that this is the right time to put forth a systematic perspective on the status of the fault-tolerant research. Altogether, this paper presents a comprehensive overview of the fault-tolerant techniques in the case of power semiconductor failures. Section II introduces general classification of conventional fault-tolerant techniques and the relevant assessment criteria. Several existing methods for the hardware fault-isolation are presented and compared in Section III. Section IV summarizes switch-level hardware reconfigurations. Leg-level and module-level for hardware reconfigurations are presented in Section V and Section VI, respectively. Section VII introduces system-level solutions. The concluding remarks and discussion are summarized in Section VIII.

II. GENERAL CLASSIFICATION

The prevailing fault-tolerant methods for power electronics converters are presented in Fig. I, which are categorized into switch-level, leg-level, module-level and system-level.

![State-of-the-art fault-tolerant methodology chart](image)

Fig. 1. State-of-the-art fault-tolerant methodology chart

Most of multilevel converters are considered switch-level redundant circuits, since some switches are added compared to basic 2-level converters. Consequently, an inherent redundancy that multiple switching combinations of three-phase correspond to the same three-phase outputs is formed. Therefore, the fault-tolerance can be realized by exploring these inherently redundant switching states [18]-[32]. The second solution for the switch-level reconfiguration is to connect the faulty converter to the midpoint of the DC-bus via additional auxiliary switches [33]-[57]. The two-phase control are normally applied in the remaining two phases to maintain balanced outputs during post-fault operations. Another scenario comes from the use of redundant switches in parallel or series connection to main switches [58]-[63]. Based on whether or not the redundant switch is operated in normal conditions, two schemes are developed: online strategy and offline strategy.

As for leg-level scenarios, a powerful solution currently in use is to apply extra legs in parallel with main legs. Since the redundant leg can substitute the damaged leg, the normal behavior of the converter can be guaranteed after faults [64]-[70]. Alternately, the redundant legs can be in series connection to the main legs for fault reconfigurations [71]-[74]. Similar to switch-level solutions, the redundant leg can be designed for online mode or offline mode based on different applications.

Module-level solutions are primarily for CMCs or MMCs. The first strategy is neutral-shift method. After faults, the number of the operative modules in each phase is unequal; the phase shifts among three phase-voltage references is adjusted to maintain balanced line-to-line voltages [75]-[82]. Another technique is the DC-bus voltage configuration method, which attempts to sustain an unchanged output voltage by raising the input voltage. The increased voltage can be normally shared by three phases via combining the neutral-shift scenario [83]-[86]. A more powerful solution currently in use is to apply extra modules in series with other modules. The redundant module substitutes the damaged one, maintaining the original outputs [87]-[88]. Similarly, the redundant module can be designed for online- or offline-mode based on applications.

More costly techniques, such as using an extra converter reserved for system fault-reconfigurations have been employed in industrial applications. Two common topologies are the cascaded redundant converter and the parallel redundant converter [89]-[95]. The additional converter can be operated in either cold or hot backup mode.

In order to assess the above techniques, the comparison criteria used in this paper are presented as follows.

1) Cost. The cost will increase if extra fuses or devices are added for system fault-tolerance. Furthermore, semiconductor devices in some basic topologies may need to be overdesigned for fault-tolerant operation, which increases costs as well.

2) Output performance. The output capability should be evaluated first. Also, other factors, such as the total harmonic distortion (THD) of output voltages or currents, system efficiency, and dynamic response should be taken into consideration as well. A topology with full fault-tolerance should behave after faults identically to normal operations.

3) Reliability. How many types of faults are covered and how much reliability is enhanced are also important metrics used to evaluate overall performance of fault-tolerant topology.

III. FAULT ISOLATION TECHNIQUES

For most of fault-tolerant solutions, the physical fault-isolation is the first step, especially in the case of short-circuit fault. The fault-isolation unit forces damaged switches or poles to be electrically isolated from the system first which can eliminate its influence over the system behavior. Then the post-fault reconfiguration can be activated. The following requirements should be taken into consideration for the design: 1) Rapidity. 2) Fault coverage. 3) Precision. The excellent isolation scheme should only isolate damaged components,
while leaving all the healthy switches operational. 4) Impact on the normal operation of the system. 5) Complexity and cost.

Fig. 2 shows five typical isolation schemes. Although these schemes are based on two-level circuits, the concept can be generally applied to other topologies as well.

Strategy 1 is shown in Fig. 2(a) [13]. This method can disconnect either a single switch or entire phase-leg from the system. For instance, \( S_1 \) isolation is implemented by triggering the semiconductor-controlled rectifier (SCR) \( T_1 \) which creates a shoot-through loop across the DC-bus and blows the fuse \( F_3 \). Note that the size of auxiliary capacitors is critical to the duration of the fault-isolation process. The main disadvantages of this strategy are as follows: 1) The presence of the fuses in the DC-bus side will increase the parasitic inductance. 2) The component count is relatively high, increasing the system cost.

Strategy 2—a simplified version of Strategy 1—has only two fuses and one triode for alternating current (TRIAC) incorporated and is shown in Fig. 2(b) [14]. Here, in the case of \( S_1 \) short-circuit, \( S_2 \) is blocked and \( T_6 \) is triggered to clear the fuse \( F_1 \). However, this strategy still has the drawback of increased parasitic inductances.

Strategy 3 is presented in Fig. 2(c). In order to eliminate the parasitic inductance due to the added fuses, the fuses are removed to the output of each phase [15]. Since the fuses are in series with output filter inductors, the effect of parasitic inductances is not important. When a short-circuit fault occurs in one of the switches, the complementary switch is blocked and the TRIAC is triggered on. Consequently, the fuse can be cleared. Still, the main drawbacks are as follows: 1) It cannot handle the fault where two switches in one pole fail simultaneously. 2) This approach isolates the whole leg, even if just one switch fails. That means, as long as one switch fails, the healthy switch in the same leg cannot continue operating.

Strategy 4 is shown in Fig. 2(d). Here, the fuse in strategy 3 is replaced by a controllable switch [16]-[17]. The switch can be relays, TRIACs or bi-IGBTs. Compared to fuses, these switches increase costs and losses. Also, different switches have special characteristics to accommodate. For instance, the time response of relays is slow. The turn-off process of TRIACs is uncontrollable and the overload capability of IGBTs is low [17]. Additionally, this approach still cannot handle the fault of simultaneous two-switch failure.

Strategy 5 is presented in Fig. 2(e). Recently, new power switches with high short-circuit capabilities and fast fuses have been developed. With the help of such power devices, it is possible to implement a simple isolation [14]. When a short circuit occurs in either one of the switches, the complementary switch is turned on to cause a shoot-through loop, blowing out the fuses. Still, the parasitic inductances of fuses exist.

IV. FAULT-RECONFIGURATIONS: SWITCH-LEVEL

After the fault-isolation, fault reconfiguration is activated. This process relies on hardware redundancy design and corresponding fault-tolerant control. This section introduces three types of switch-level hardware redundancies and associated control strategies.

A. Redundant Switching States

Multilevel converters are in essence one type of switch-level redundant circuits, where some switches are added into basic 2-level converters. Due to these additional switches, the redundancy of output switching states is created. Therefore, the fault-tolerance can be realized by exploring these redundant switching states. Note that the method is normally implemented based on the space-vector modulation (SVM) algorithm [18]-[19].

Li et al. proposed a control scheme of utilizing the voltage vector redundancy for neutral-point clamped (NPC) inverters [20]. Assuming that \( S_{al} \) fails in short-circuit, phase-A cannot output zero-level due to the shoot-through path as shown in Fig. 3(a). As a result, the voltage vectors involving zero-level of phase-A are invalid as shown in Fig. 3(b). The converter is still able to output a full voltage with the help of redundant vectors. However, the other issues are introduced [21]. Specifically, \( S_{al} \) has to withstand the total dc-bus voltage, which leads to the oversized design of the semiconductors. A similar approach is applied in other 3-level topologies, like T-type [22], active NPC [23], etc. It is worth mentioning that, when the middle switches fail in open-circuit in T-type three-level converters, it can be degraded into two-level without any loss of output voltage.

The fault-tolerant operation based on the vector redundancy is also employed in CMCs [24]-[25]. When some switches in the circuit fail, the corresponding space vectors become invalid and the output voltage is decreased. In [26], the faulty cells also participate in the operation and contribute output levels depending on specific faulty switches. In addition, in order to solve the computational complexity with the increase of number of modules, the space vectors are defined in a 60° \( g-h \) coordinate system [27]. Based on the 60° \( g-h \) coordinate system, a pulse width modulation (PWM) pattern called large-small alternation (LSA) is proposed [28]-[30]. Compared to other methods, the LSA modulation results in output line-to-line voltages with the lowest THD in the post-fault [28].
Note that this inherent redundancy exists in not only 3-phase switching combinations, but also switching states of a single phase in some converters. For instance, in multilevel active clamped (MAC) converters, when the output is 1Vdc, two conduction paths can be selected as shown in Fig. 4(a), which can be utilized for redundancy [31]. However, it implies an increase of the blocking voltage of some devices in some fault conditions. For instance, Sn33 has to withstand 2Vdc when the output level is 3Vdc in the case of Sn23 short-circuit (see Fig. 4(b)). Alternatively, a scheme is proposed [31] to maintain the original device blocking voltage but at the expense of some output levels.

![Fig. 4. Multilevel active clamped topology (a) Output is 1Vdc (b) Sn33 overvoltage when Sn23 is short-circuit](image)

In order to further improve the fault-tolerance, some auxiliary switches are added, which increase the number of redundant switching states. Fig. 5(a) presents a modified 5-level MAC topology [31], where two auxiliary devices are added at terminals #2 and #4. A similar approach is applied in general multilevel converters proposed by Chen et al. [32]. This method can tolerate any single device failure without loss of any output-voltage levels. Nevertheless, the main disadvantages lie in these aspects. 1) An increased number of conduction devices lead to higher conduction losses. 2) The blocking voltage of some devices is unavoidably doubled. For instance, when Sn33 fails in short-circuit, Sn22 has to withstand 2V shown in Fig. 5(b). 3) The modified architecture loses the features of good symmetry compared to the original circuit.

![Fig. 5. Fault-tolerant multilevel active clamped topology (a) Normal Operation (b) Output is 0V in the case of Sn33 short-circuit failure](image)

In summary, the main disadvantages of redundant switching states approach are as follows.

1) The performance in post-fault operations is degraded. Either the output voltage is reduced, or the blocking voltage of devices is increased, or suboptimal output THD occurs.
2) The fault coverage of this approach is limited.
3) The approach utilizing 3-phase redundant vectors can only be employed in a three-phase three-wire system.

**B. DC-Bus Midpoint Connection**

As for three-phase converters, if one phase fails, the remaining two phases can maintain continuous operations. Three typical fault-tolerant topologies with additional switches employed in motor applications are presented in Fig. 6 [33].

![Fig. 6. Switch-level fault-tolerant motor drives (a) Topology 1 (b) Topology 2 (c) Topology 3](image)

The first fault-tolerant topology shown in Fig. 6(a) forces the faulty phase to connect to the midpoint of the DC-link via the additional TRIACs [15], [34]. After faults, the reconfigured system is similar to the structure where only four switches are used to drive a three-phase machine [35]. Note that since the inverter is still capable of providing the full rated current, the torque production will be preserved. Nevertheless, the main disadvantages are as follows.

1) The maximum balanced line-to-line output voltage in post-fault operations is reduced to half of its nominal value.
2) This approach is only applied in situations where the midpoint of DC-link capacitors can be accessed.
3) Since the phase-current flows into the midpoint of the DC-bus, oversized DC-bus capacitors are mandatory.

The second method connects the neutral-point of the motor to the DC-bus midpoint via the incorporated TRIAC $T_N$ as shown in Fig. 6 (b) [36]-[37]. Note that only one TRIAC is added for the fault-tolerance. In case of loss of one phase (e.g. phase-A) as shown in Fig. 7(a), the magnitude of phase-B and phase-C currents is increased by $\sqrt{3}$ and the phase shift between these two is regulated to 60° in post-fault operations as shown in Fig. 7(b) [6]. Note that the modified control strategy leads to a zero-sequence current. Therefore, $T_N$ needs to be turned on after faults to flow the neutral current.

![Fig. 7. (a) Phase-A failure (b) Phasor diagram in the pre- and post-fault](image)

Nevertheless, the drawbacks of this approach can be identified as follows.

1) The oversized semiconductors are necessitated.

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2) The maximum speed of the machine in post-fault is reduced to 0.5 of its nominal value because the equivalent line-to-line voltages are decreased to 0.5pu.
3) This approach can only be applied when the DC-bus midpoint and the motor neutral-point can both be accessed.
4) The neutral-current is significantly increased, which necessitates oversized DC-bus capacitors.

The third method connects the neutral-point of a motor to an additional fourth leg [38]-[39]. As shown in Fig. 6 (c), an extra leg and a TRIAC are incorporated. It is worth mentioning that the fourth pole can be permanently connected to the converter even in normal operations without TRIACs [38]-[39]. Compared to the previous two solutions, this topology yields the following good features.

1) The system is free of the DC-bus midpoint balancing problems and minimum capacitance sizing.
2) The line-to-line voltage can be increased to 1pu compared to previous methods.

A similar principle can be applied in five-phase motors as shown in Fig. 8. However the solution for generating the unchanged rotating magneto motive force (MMF) is not unique. Normally, two strategies are employed [40]-[42], (see Fig. 8(b)-(c)). In the first scheme, there is an attempt to generate the unchanged rotating MMF with the minimum possible current magnitude of the remaining healthy phases. All the current references are increased by 1.314 times and shifted by 18 degrees as shown in Fig. 8(b). However this solution exhibits a zero-sequence current component. In the second strategy, the current references of the healthy phase are modified to achieve undisturbed MMF and eliminate zero-sequence current components. In this case only two current reference vectors are rotated by 36 degree (see Fig. 8(c)). However, the magnitude of the remaining phase has to increase by 1.38 times to achieve the unchanged MMF. A similar approach can be applied in other multi-phase motors, like six-phase [43], four-phase [44], etc.

Fig. 8. Five-phase machine (a) Phase-A failure (b) Strategy 1 in case of phase-A failure (c) Strategy 2 in case of phase-A failure

The disadvantages of this approach in motor applications are as follows.
1) The method only can handle open-circuit failures happening in the signal-phase or multiple phases.

2) Since the healthy phases have to withstand over-current after faults, oversized devices are necessary. Also, the over-current is decreased with an increase of the phase number.

3) For a three-phase machine, a neutral connection is necessary. If the neutral current flows into the DC-bus, it necessitates oversized capacitors.

A similar idea can be applied in 3-phase voltage source inverters (VSIs). As shown in Fig. 9(a), the basic idea is to constantly force the output voltage of the faulty phase to zero and regulate the phase-angle of the other two phase voltages, maintaining balanced line-to-line voltages in post-fault. As shown in Fig. 9(b), the phase angles of phase-B and -C will be shifted by 30° away from the faulty phase (phase-A) [19]. Note that the equivalent balanced phase-voltages in post fault conditions (\(v_{AE}', v_{BE}', v_{CE}'\)) are only \(1/\sqrt{3}\) of those in normal conditions as shown in Fig. 9 (b).

Fig. 9. Two-phase control in voltage source inverters (a) Phase-A failure (b) Phasor diagram in the pre- and post-fault

Following a similar approach, TRIACs are added to 6-leg AC-DC-AC converters [45], 5-leg converters [46], nine-switch converters [47], and matrix converters [48]-[50] for fault-tolerance. Note that the matrix converter is treated as a two-stage rectifier/inverter [51]-[52]. The existing modulation techniques for the inverter stage can be used. As for multilevel converters, an additional TRIAC \(T_{X}\) is employed in NPC converters to connect the output to the mid-point as shown in Fig. 10(a) [20], [53]. An alternative scheme is the active-NPC topology as shown in Fig. 10(b) [23], [54], which utilizes IGBTs to replace clamped diodes, such that the output terminal of the faulty phase can be connected to the mid-point via \(S_{y}/S_{z}\) or \(S_{y}/S_{x}\). However, the output voltages in these two approaches are both reduced after faults. In an attempt to overcome this problem, some fast fuses and thyristors are added as shown in Fig. 10(c) [55]-[56]. In case of a short-circuit fault, the corresponding thyristor is triggered to clear the associated fuse. Consequently, the faulty leg is reconfigured into a two-level structure. However, some semiconductors have to withstand overvoltages. A similar approach is applied in active-NPC [55]-[56] shown in Fig. 10(d). Due to the additional switching states provided by the extra switches \(S_{y}/S_{x}\), the faulty leg is still able to achieve three voltage levels in some fault conditions. However, the main drawback remains the oversized semiconductors.

In additional, Ma et al. applied the two-phase control in general multilevel converters, which combined dc-component injection as well [57]. However, the reduced output voltage is still the primary issue during post-fault conditions.
C. Redundant Parallel or Series Switches Installation

1) Redundant Parallel Switch

This approach places extra switches in parallel with the main switches. Based on whether or not the redundant switch is operated in normal conditions, this method is implemented in two ways: offline scheme and online scheme.

In the offline scheme, the redundant switch is not operated in normal conditions. When a fault occurs, the redundant switches are activated to replace faulty switches. As shown in Fig. 11(a), the traditional MC is accompanied by a bidirectional switch and a series of relays [58]. The redundant switch can replace any of the switches via selecting relays. In order to increase the system availability, more redundant switches can be added [58]. A similar approach is introduced into two-level inverters [59]. Thyristors can replace relays to reduce the transition time due to their short turn-on time.

2) In the offline scheme, one redundant unit is shared by multiple main switches, which can reduce the system cost. However, more linking switches are introduced.

3) In the offline scheme, the linking switches increase the conduction loss in post-fault. In the online scheme, the parallel switches can reduce conduction losses in normal conditions.

2) Redundant Series Switch

The two-level voltage source converter with IGBTs directly in series is widely used in flexible HVDC transmissions [60]. The redundant devices are connected in series with main switches for short-circuit failures as shown in Fig. 12(a) [61]. The overall conduction losses are doubled in normal operations. Also, the voltage sharing issue among the series devices has to be addressed. In addition, some switches have to withstand overvoltages after short-circuit failures. In order to further handle open-circuit failures, this topology is modified by adding parallel thyristors as shown in Fig. 12(b) [62]. However, this scenario is at the expense of higher costs.

Another topology providing the series redundancy is flying capacitor multilevel converters (FCMCs). As shown in Fig. 12(c), an fault-tolerant design for three-cell 4-level FCMC is proposed in [62]-[63]. When a single-switch fault occurs, the faulty switch and its counterpart are bypassed. The corresponding capacitor is isolated from the system or constantly connected in parallel with another capacitor. However, the primary disadvantages are the following.

1) Some switches need to withstand the full DC-link voltage after failures.

2) The series switches \( K_f, K_s \) experience on-state losses during normal operations.

V. FAULT-RECONFIGURATIONS: LEG-LEVEL

In this section, two types of leg-level hardware redundancies and associated control strategies are introduced, which are redundant parallel leg and redundant series leg.

A. Redundant Parallel Leg

This approach is implemented via adding a parallel redundant leg. Depending on whether or not the redundant parallel leg functions in pre-fault, there are two schemes: offline leg scheme and online leg scheme.

Fig. 13(a) presents a solution based on an offline parallel leg [64]. Since the number of the redundant leg is only one, three main legs share it together which reduces the entire cost.
Meanwhile, three TRIACs, e.g. $T_a$-$T_C$, are added as linking switches. Before faults, the additional leg is inactive. When a fault occurs, the spare leg replaces the faulty leg. Note that the topology can only cover the fault happening in a single phase. A similar approach is applied in doubly fed induction generator (DFIG) systems [65] and HEVs [16], [66]. It is observed that multiple converters share one redundant leg to reduce system costs. In order to increase the system availability, the number of the redundant legs is increased up to three [61] as shown in Fig. 13(b). Since relays have a considerable amount of delay, they can be replaced with bidirectional switches to shorten the dynamic process [67].

![Fig. 13. Offline parallel redundancy leg solutions (a) One redundant leg (b) Three redundant legs](image)

In the online leg scheme, the redundant leg operates even in normal conditions to improve the system behavior. Two modified topologies based on the 3-level NPC topology are presented in Fig. 14 [68]-[70]. Taking the circuit in Fig. 14(a) as an example, the fourth leg adopts a flying capacitor topology different from the main legs. In normal conditions, this additional leg provides a stiff neutral-point voltage. When a fault occurs (e.g. phase-A), the fuses $F_a$ and $F_b$ are blown out first. Then, $S_{R5}$, $S_{R6}$ and $T_a$ are activated. Consequently, the faulty leg is substituted by the fourth leg and the system is reconfigured as a standard NPC converter. A similar principle can be applied in the circuit in Fig. 14(b).

![Fig. 14. Online parallel redundancy leg topologies (a) Flying capacitor redundant leg (b) Inductor redundant leg](image)

To sum up, the principle features of the parallel leg approach are identified as follow.

1) The number of the redundant legs can be from 1 to 3. The number is a balance of offsetting the improved reliability with the increased costs.

2) In the offline scheme, the linking switches are required. The added linking switches increase the conduction loss in post-faults. Therefore, it is significant to apply semiconductors with a lower on-state resistance as the linking switches.

3) The topology of the redundant legs could be the same, or different, as that of legs in the original circuit. Hence, it can select its own topology based on the specific requirements.

4) The backup leg can operate in online or offline mode. The loss is higher in the online mode due to the fact that the additional leg is operating. However, the online backup leg can help improve the output quality in normal conditions.

### B. Redundant Series Leg

The series redundancy leg is widely applied in 3-phase motor drives [71] as shown in Fig. 15(a). Note that the voltage space vectors are the same as 3-level inverters [72]. In case of short- or open-circuit failures, the faulty leg stops working, while the two remaining phases continue operating to maintain the original flux. However, the output voltage is reduced during post-fault operations. Therefore, an alternative configuration using the same number of switches with two isolated and unequal dc-link voltages ($V_{dc1}$, $V_{dc2}$) is reported as shown in Fig. 15(b) [73]-[74]. The output capability of the system can be increased to some extent. However, the oversized semiconductors are still necessitated.

![Fig. 15. Series redundancy leg solutions (a) Topology 1 (b) Topology 2](image)

### VI. FAULT-RECONFIGURATION: MODULE-LEVEL

CMCs and MMCs are typical circuits with module-level redundancy. If some modules fail, the other modules implement the fault-tolerant reconfiguration to maintain continuous operations. The main approaches are neutral-shift, dc-bus regulation and redundant module installation.

#### A. Neutral-Shift

After faults, an unequal number of modules are applied in three phases. Therefore, this method is attempted to modify phase shifts among phase-voltage references to maintain balanced line-to-line voltages in post-fault. It functions as though the equivalent neutral-point is shifted after faults, so it is called neutral-shift (NS) method. 

Taking the 5-module 11-level CMC as an example, when a fault occurs with two faulty modules in phase-$b$ and one faulty module in phase-$c$, the unbalanced line-to-line voltages are applied. To keep balanced line-to-line voltages, the simplest solution is to bypass an equal number of modules per phase as shown in Fig. 16(a) [75]. However, this approach results in very low output voltages. Therefore, [76] introduces the NS method to maximize the line-to-line voltages, where the angles of the phase voltages are recalculated after faults. The phase-shift angles for different faults [77] are

$$
\begin{align*}
V_3^0 &+ V_3^0 - 2V_c^0 \cos(\alpha) = V_3^0 + V_3^0 - 2V_c^0 \cos(\beta) = V_3^0 + V_3^0 - 2V_c^0 \cos(\gamma)
\end{align*}
$$

$$
\alpha + \beta + \gamma = 360^{\circ}
$$

(1)
where $V_a$, $V_b$, $V_c$ are the magnitudes of three phase voltages, and $\alpha$, $\beta$, $\gamma$ are the angles between every two phase-voltages.

In summary, the NS method is easy to be implemented. Nevertheless, the primary disadvantages are as follows.

1) This approach cannot be employed in the application of three-phase 4-wire systems.
2) The full voltage in normal situations still cannot be achieved during post-fault conditions.
3) In post-fault conditions, the load power factor not only depends on the load characteristic, but also on how much the neutral-point is shifted.

Since the injected zero-sequence component is all fundamental frequency, the NS method limits the range of load power factor [82]. Therefore, some alternative zero-sequence component injection methods with non-fundamental frequency based on the carrier-PWM are proposed to eliminate the adverse effect of the NS method [80]-[81]. Furthermore, Carciulitti et al. analyzed a formal mathematical derivation to establish a theoretical background [82]. For a given fault condition, the optimum zero-sequence components for the output line-to-line voltages are obtained. However, the process of obtaining the zero-sequence component in this method is relatively complex.

B. DC-Bus Voltage Reconfiguration

It is noted that a common drawback of the previous method is the reduced output voltage during post-fault operations. Therefore, in an attempt to sustain an unchanged output voltage, an alternative approach is to increase the input DC-bus voltage. The DC-bus voltage reconfiguration is generally categorized by whether the overvoltage is withstood only by the faulty phase or shared among three phases.

In applications of static compensators [83]-[84], H-bridge modules in a CMC are used as active rectifiers. When the faults occur, the DC-link voltages of the remaining modules in the faulty phases are increased to keep the total voltage unchanged. For example, in the case of the fault as in Fig. 19(a), the voltage stress on remaining semiconductor devices is increased by 200% (shown in Fig. 19(b)).

Unlike the previous method, the approach in [84]-[85] introduces a neutral shift, sharing the increased voltage burden equally among all healthy modules of three phases. As shown...
in Fig. 19 (c), the DC-link voltage of the remaining modules is only increased by 35% with this method.

Although the output voltage can be sustained at same level as that in the pre-fault condition, the principle drawbacks of the DC-bus voltage reconfiguration still exist as follows:

1) The increased DC-bus voltage can expose a higher voltage stress on the devices, necessitating oversized design.

2) The combination of the DC-bus reconfiguration and neutral-shift can only be applied in three-phase 3-wire systems.

Moreover, another post-fault reconfiguration to maintain output voltage is realized by regulating the output transformer turn ratio [86]. This reconfiguration method is based on a multi-coil transformer and a set of bidirectional valves for the system fault-tolerance. However, the added hardware increases the system costs greatly.

C. Redundant Modules Installation

For CMCs, redundant modules are added in series with the basic topology as shown in Fig. 20(a). Normally, the redundant modules are inactive. When any module has a fault, it will be isolated by setting the bypass switch $T$ in the “3-4” position. Subsequently, the redundant module starts to replace the faulty module and reestablish the normal operation. The bypass switches can be simplified by applying the failure characteristics of semiconductors. In contrast, in [83], the redundant modules are active in normal operations. Therefore, the output quality is improved compared to the previous method. However, the conduction losses are relatively higher. The fault-tolerant control is shown in Fig. 20(b). It can be seen that the output voltage amplitude of the each cell in faulty phase is increased after faults. A similar approach can be applied in MMC [87]-[88], shown in Fig. 20(c). The redundant modules adopt the online mode, which can reduce the transition time and the charge time of redundant modules.

![Diagram](image_url)

Fig. 20. Series redundant module (a) Cascaded converters topology (b) Cascaded converters control (c) modular multilevel converters topology

VII. HARDWARE RECONFIGURATIONS: SYSTEM-LEVEL

In this section, two types of system-level hardware solutions for fault reconfiguration are introduced, which are cascaded converters and parallel converters. As shown in Fig. 21(a), three switches are added in series with each output phase [6]. Therefore, the modified configuration is able to handle single switch short-circuit, single switch open-circuit, and phase-leg open-circuit. However, the power rating after faults is degraded. Parallel converters have been used to improve the reliability in active power filters [89], uninterruptible power supplies (UPSs) [90], and DFIGs [91]. As shown in Fig. 21(b), one of inverters is operated in normal condition. When faults occur, the other inverter can replace the faulty one for continuous operation. However, when the dual converters are operated at same time during normal situations, the reduction of circulating currents among converters is an important objective to address. Several control techniques have been developed to ensure equal load sharing [92]-[93]. As shown in Fig. 21(c), the current sharing is controlled via regulating the magnitude and the phase angle of the output references. In addition, this concept is applied in DC/DC converters, AC/DC converters, etc. Two common connection structures are common DC-bus and high frequency AC-bus.

![Diagram](image_url)

Fig. 21. (a) Series converters for motor drive (b) Parallel converters for UPS system (b) Control strategy for parallel UPS system

VIII. CONCLUSIONS

This paper presented a comprehensive review of fault-tolerant techniques in power electronic converters that have been introduced in past literatures. The fault-tolerant solutions are always based on hardware redundancy plus associated control strategies. Therefore, the conventional fault-tolerant techniques are classified into switch-level, leg-level, module-level and system-level solutions based on the type of hardware redundancy. Various approaches are presented and their advantages and disadvantages are analyzed in detail. It is shown that some fault-tolerant methods, such as redundant switching states and neutral-shift, are easily implemented and cost-effective, but cannot maintain the full rated power after faults. Therefore, in mission critical applications, the full fault-tolerant design serves as a more suitable option. Therefore, multiple modified topologies with full fault-tolerant capability are summarized. Among them, the redundant parallel leg topology is recognized as the optimal compromise between system cost, performance and reliability. Additionally, the implementation of redundant parallel...
converters is a relatively mature technique, widely employed in industrial applications. In conclusion, the past research identifies the following key results and limitations.

1) As for fault-isolation circuits, the elimination of increased parasitic inductance due to the presence of fuses needs to be studied further. Development of power switches with better short-circuit capabilities and faster fuses would greatly simplify the fault-isolation circuit.

2) The combination of connecting the faulty leg to the DC-bus mid-point and two-phase control are widely applied in motor drives, which can optimize the redundancy design. Therefore, it is beneficial to further investigate the hardware and software combination technique for system fault-tolerance.

3) The parallel and series redundant switch, leg or module is a big branch of the hardware fault-tolerant solutions. The redundant unit can be designed in online or offline mode. Present attention is directed to the offline leg structure due to remarkably better performance and relatively lower cost. Additionally, the redundant module applied in MMC for system redundancy is an hot area of present research.

4) The solutions utilizing the inherent redundancy such as redundant switching state and neutral-shift are similar in nature, but differ in the implementation and the form of the zero-sequence component. Therefore, these approaches cannot be employed in a three-phase four-wire system due to the injected zero-sequence component. Also, the reduced output voltage in post-fault condition is the common drawback for these strategies.

5) The DC-bus voltage reconfiguration method necessitates oversized semiconductors, limiting its application range. It is significant to note that the future direction should look to explore the combination of multiple methods to optimize fault-tolerant performance.

6) Very few literatures quantitatively analyze the transition from the faulty state to the post-fault state. How to achieve the seamless and rapid transient processes from fault occurrence to post-fault operation should be addressed further.

7) Since most of the fault-tolerant strategies are only feasible for single open- or short-circuit fault, the fault-tolerant topologies designed to handle multiple faults is quite few. Further investigation into methods capable of handling multiple simultaneous faults is needed.

8) Very few quantitative reliability estimations on topologies after redundant design are reported. It is important to form systematic approaches to assess the reliability of fault-tolerant design.

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