DESIGN OF 16-BIT MULTIPLIER USING MODIFIED GATE DIFFUSION INPUT LOGIC

G.VIJAYA KUMAR[1]
gollavijayakumar459@gmail.com

P.KRISHNA REDDY[2]
Krishna.papana@gmail.com

[1]PG Student Dhanekula Institute of Engineering and Technology Ganguru, Vijayawada.
[2]Assistant Professor, Dept. of ECE, Dhanekula Institute of Engineering and Technology Ganguru, Vijayawada.

Abstract— Now a day the growth of the electronic market, VLSI industry has driven towards the very high integration density. While integration density on a chip increases, critical concerns arises regarding the size and power dissipation of the components on the chip. In the recent years, various effort has been made for reducing the area, power consumption of the components as well as for reducing the propagation delay of them, such as scaling and different topologies like pass transistor logic (PTL), Transmission gates etc. One such topology is Gate Diffusion Input (GDI) technique which is used in the present design. Multiplication acts as an important part in high speed digital signal processing. It is the most important module of various arithmetic and logical units such as ALU and ASICs where high processing speed is needed. The Modified Gate Diffusion Input (MGDI) logic reduces the area of digital circuit while designing the digital circuits. In this Modified Gate Diffusion Input (MGDI) logic technique is used for design of 16-bit multiplier by performing multiplication operation on unsigned numbers. The main modules of 16-bit MGDI multiplier architecture are two's complement generator, Booth encoder, partial product generator, Wallace tree adder and final adder respectively. The proposed MGDI designed circuits are extensively simulated on Mentor Graphics tool.

Keywords: MGDI, Booth Encoder, Partial Product Generator, Wallace Tree Adder**.**

I. INTRODUCTION

Among the forceful investigation in the field of low power, high speed digital applications due to the growing demand of systems like phones, laptop, palmtop computers, cellular phones, wireless modems and portable multimedia applications etc has directed the VLSI technology to scale down to nano-regimes, allowing additional functionality to be incorporated on a single chip. Figure 1 shows basic GDI logic cell which is used for implementing complex functions and circuits. Where G, P and N are three inputs and output is taken from D terminal.

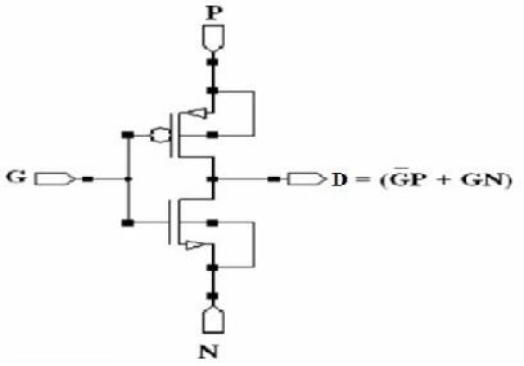

Figure 1: GDI basic cell

Advantages of GDI over CMOS

1. Low power circuit design.
2. Reducing propagation delay
3. Reducing area of digital circuit

Disadvantages od GDI:

It doesn't produce full outputp swing for all input combinations.

Modified Gate Diffusion input Logic:

It contains G,N,P,D,S_P,S_N terminals.all are input terminals except D. S_P and S_N are fixed terminals.

It is contrast wit basic GDI cell contains a low voltage terminal $S_p$it is connected to a supply voltage terminal S_n it is connected to ground.

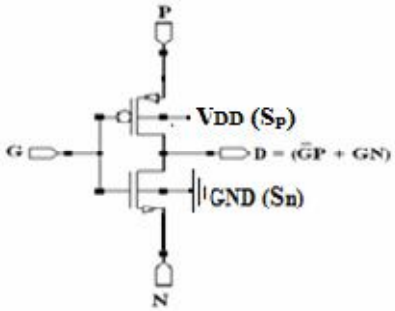

Figure 2: MGDI basic cell

N	S_N	P	sp	G	D	function
0	0	1	1	A	A`	Inv
A	A	0	A	B	AB	And
1	0	A	B	B	A+B	Or
A	0	A	1	B	A`B+AB`	Xor
A	0	A`	1	B	AB+A`B`	Xnor
0	0	B	B	A	A`B	F1
B	0	1	1	A	A`+B	F2
C	0	B	1	A	A`B+AC	mux

Table 1: Some functions are implemented in MGDI

Advantages of MGDI:

In the CMOS technology gate power dissipation and switching dissipation losses are occurred

1. Sub-Threshold Leakage
2. Gate Leakage occurred in CMOS fabrication are avoided by using MGDI.

II Architecture of 16-bit multiplier

The 16-bit Multiplier Architecture is divided into four modules and each module can be explained in the following subsections.

A. Two's Complement Generator

The signed Multiplicand (MD) can be represented in two's complement form .it can be obtained by one's complement the (MD) and adding 1 to the least significant position of the one's complement form.

Example: 6= 0110
One's complement of 6=1001
Adding 1 to LSB 1
2's complement =1010

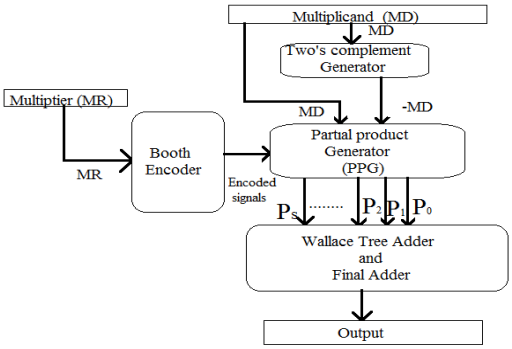

Figure 3: Block diagram of 16-bit MGDI Multiplier

B. Booth Encoder

The Booth encoder is used for reduce the number of partial products based on recoding the Multiplier (MR) in a higher radix. The number, n, of the bits inspected in radix, r, is given by

n = 1+ r, r = 4 (radix-4) (1)

n = 1 + 2 = 3

The Multiplier (MR) can be divided into overlapping groups of three bits at a time this is shown in figure 4.

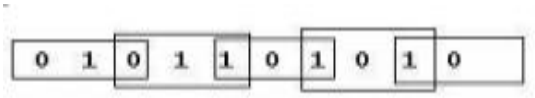

Figure 4: Grouping of triplets from the Multiplier (MR)

By using booth encoder whose functions are given in table 2.The operation –MD can be realized by the two's complement of the Multiplicand. The operations 2MD and -2MD can be realized by shifting one bit position of MD and -MD to left and filling the LSB with zero. An easier way to identify the required operation is given by formula is $-2D_2+ D1+D0$

D_2	D_1	D_0	function	neg	pos	two	one
0	0	0	+0	0	1	0	0
0	0	1	+MD	0	1	0	1
0	1	0	+MD	0	1	0	1
0	1	1	+2MD	0	1	1	0
1	0	0	-2MD	1	0	1	0
1	0	1	-MD	1	0	0	1
1	1	0	-MD	1	0	0	1
1	1	1	-0	1	0	0	0

Table2: Booth encoder

C. Partial Product Generator

Booth encoder produces the encoded signals .These encoded signals acts as selection signals which are given to partial product generator. It can be designed using 2:1 multiplexer. 2:1 multiplexer are designed using AND and OR gates. After generating partial products each partial product is shifted two bits with respect to its neighbours.

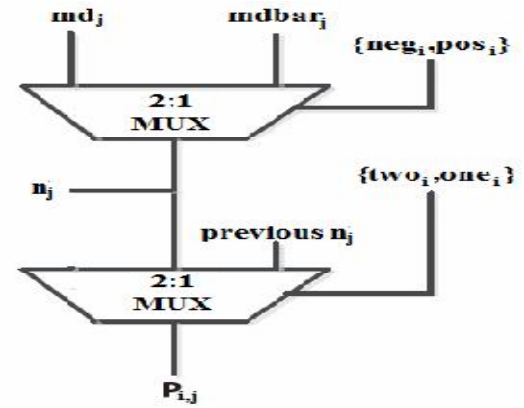

Figure: Partial product Generator for 1-bit multiplicand .

D. Wallace tree adder

The Wallace tree method is used in high speed designs in order to produce two rows of partial products that can be added in the last stage. Half adder, full adder, unit adder and carry save adders are employed in Wallace tree structure to reduce partial products. Wallace tree accelerate the accumulation of the partial products. The speed, area and power consumption of the multipliers will be in direct proportion to the efficiency of the compressor. Wallace tree adder produces 32-bit sum and 32-bit carry output.

E. FINAL ADDER

The output of Wallace tree adder given to final adder .Final adder adds sum and carry bits and produce 32-bit multiplied output. Final adder is designed using full adders and buffers.

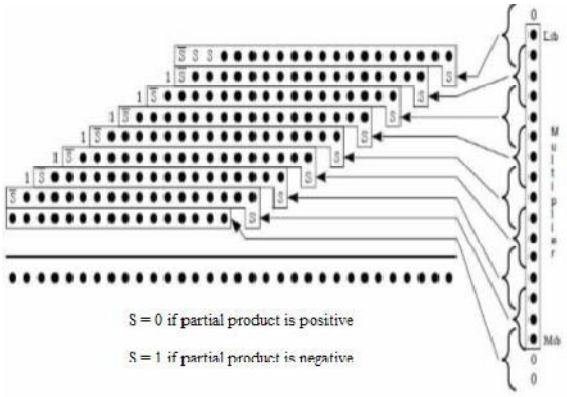

Figure 7: Dot diagram for 16-bit Multiplication

III IMPLEMENTATION OF 16-BIT MULTIPLIER USING MGDI

The 16-bit Multiplier shown in figure 3 is now designed using MGDI logic using Mentor Graphics tool. using AMI 130 nm CMOS technology at 2.5v supply voltage.
In the first step, design of basic gates, main modules like two's complement generator, partial product generator and sub modules like full adders, half adders are carried out in MGDI. These sub modules are combined in the main modules of 16-bit Multiplier design.

Design of basic gates (AND, OR) and XOR gates in MGDI logic:

The two input AND & OR gates are implemented in Modified Gate Diffusion Input (MGDI) logic and to avoid the swing degradation. The schematic of these gates are shown in figure 8 & figure 9 respectively. Inverters are used for the complement of inputs. Buffers are in build of inverters and to improve ability of outputs. Also, XOR gate realized as shown in figure 10.

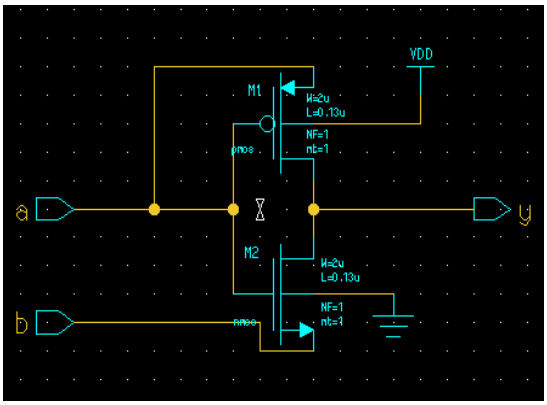

Figure 8: Schematic of two input MGDI AND gate

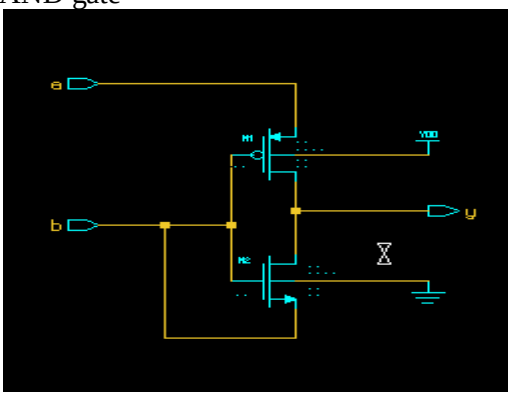

Figure 9: Schematic of two input MGDI OR gate

The sub modules are designed by using above gates. Like half adder is implemented as sum, carry using XOR gate and AND gate respectively.

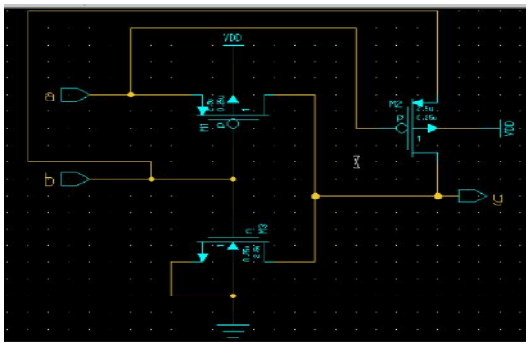

Figure 10: Schematic of two input MGDI XOR gate

Full adder is implemented as sum, carry using XOR gate, inverter and two transistors of two 2:1 multiplexers shown in figure 11.

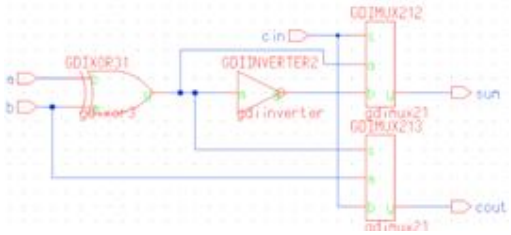

Figure 11: Schematic of MGDI Full adder

The design of 16-bit Multiplier is made by combining these sub modules to improve the main modules such as Booth encoder, Two's complement generator, Partial product generator, Wallace tree adder and Final adder. The schematic of these main modules are as shown in figure 12, figure 13 and figure 14.

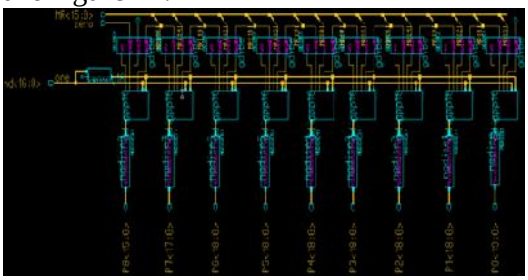

Figure 12: Schematic of Partial product generator along with Booth encoder and Two's complement generator

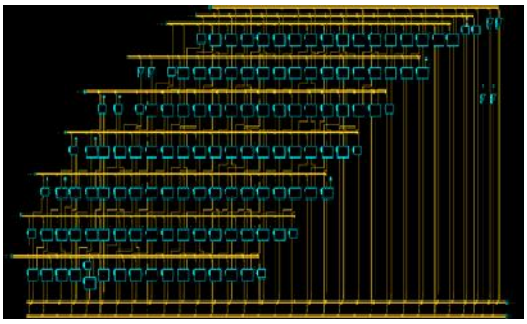

Figure 13: Schematic of MGDI Wallace tree adder

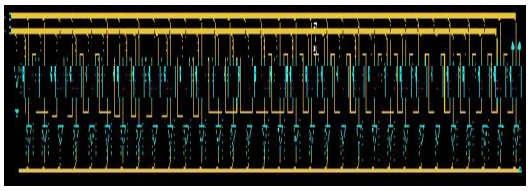

Figure 14: Schematic of MGDI Final adder

The final 16-bit Multiplier is implemented by using combining the main modules as indicated in figure 3. The final schematic of 16-bit Multiplier is shown in figure 15.

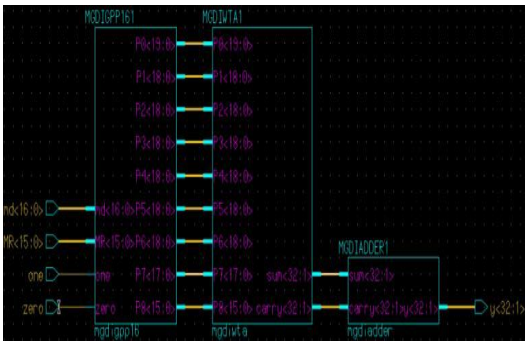

Figure 15: Schematic of Final 16-bit MGDI Multiplier

IV SIMULATION RESULTS AND COMPARATIVE STUDY OF THE 16-BIT MULTIPLIER DESIGN

The Schematic of Multiplier is designed using Mentor Graphics tool using AMI 130 nm CMOS technology at 2.5v supply voltage. figure 16 shows simulation results for input Multiplicand $(45671)_{10}=(0101100100110011 1)_2$and Multiplier $(38503)_{10}= (1001011001100111)_2$and its Multiplied output is $=(1758470513)_{10=}$ $(01101000110100000010000101110000)_2$

Sl. No.	Gates/Adders	Devices in CMOS	Devices in GDI	Devices in MGDI
1	Inverter	2	2	2
2	Two input AND Gate	6	5	2
3	Two input XOR Gate	12	8	3
4	Two input OR Gate	6	4	2
5	Half Adder	18	13	5
6	Full Adder	42	32	9

Table3. Comparison of CMOS,GDI,MGDI (Radix-2) had some drawbacks such as

1. More number of partial products are generated
2.It is becomes inefficient when there are isolated 1's.

Sl.No.	Main Modules	Number of devices in CMOS design (radix-2)	Number of devices in GDI (radix-2)	Number of devices in MGDI (radix-4)
1	Two's complement generator	320	240	119
2	Booth encoder	318	238	153
3	Complete partial product generator	9888	8864	2808
4	Adder circuit	14740	11220	1536
5	Final 16-bit Multiplier	25266	20562	4344

Table 4. Comparison of 16-bit multiplier in radix 2 and radix 4

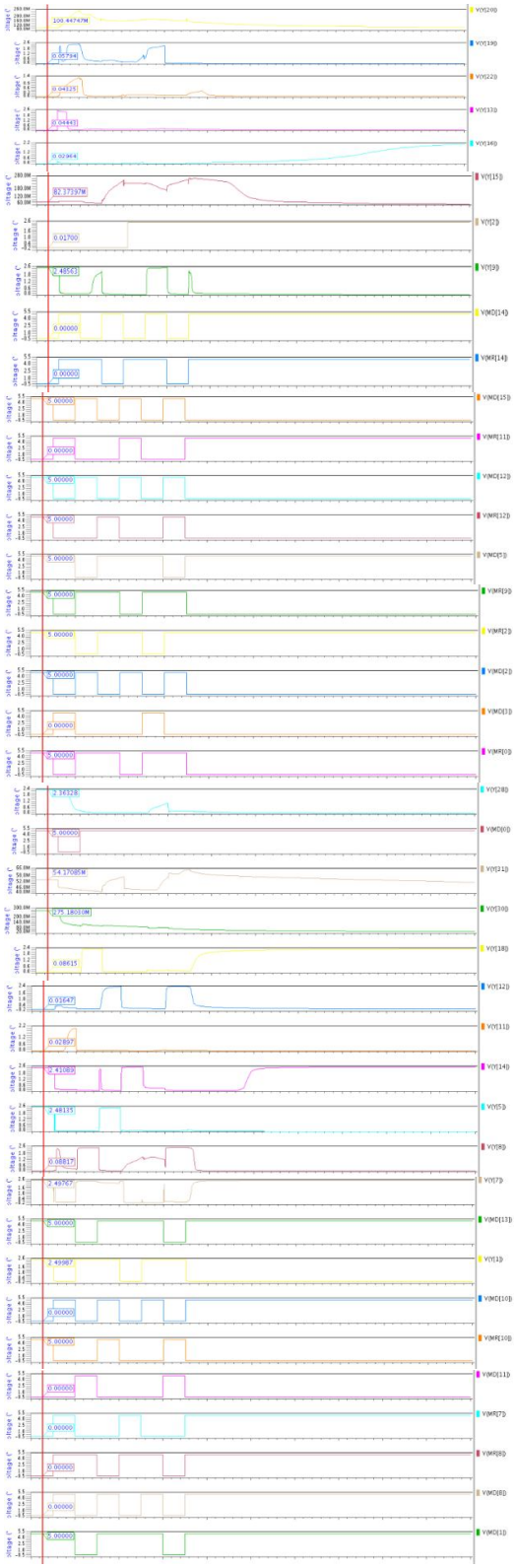

Fig 16: simulation results of 16-bit MGDI multiplier

In Radix-4 system number of partial products are reduced compared to the Radix-2 system.

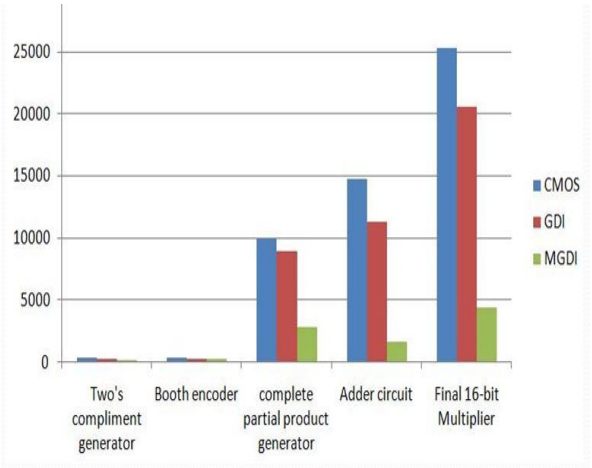

Fig: Graphical representation of CMOS,GDI,MGDI

CONCLUSION

The 16-bit Multiplier is designed in MGDI logic in Mentor Graphics tool .The Multiplier design in MGDI is to show reduction of number of transistors in the Multiplier design compared to CMOS and GDI designs. A comparative study is made regarding the total number
of devices required for the Multiplier design using CMOS, GDI and MGDI logics. It is observed that Multiplier designed in MGDI results in reduction of devices, thus minimizing the area of Multiplier.

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Mr. P.Krishna Reddy was born in A.P, India in 1987. Completed M.Tech in VLSI Design at SRM University Chennai and B.Tech from Laki Reddy Bali Reddy college of Engineering Mylavaram affliated to JNTUK, in the year 2009 in Electronics and Communication Engineering. He worked as Assistant professor in PPDCET, Surampalli. Presently working as Asst. Professor in Dhanekula Institute of Engineering and Technology, Ganguru. His research interests in Low power VLSI and Embedded Systems.

Mr. G.VIJAYA KUMAR was born in Krishna (Dt),AP in 1991 .He graduated from the Sarojini Institute of Technology, Telaprolu. His special fields of interest included VLSI. Presently he is studying M.Tech in Dhanekula Institute of Engineering and Technology, Ganguru.