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Design of Low Power, High Performance 2-4 and 4-16 Mixed-Logic Line Decoders

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***Abstract*—This paper introduces a mixed-logic design method for line decoders, combining transmission gate logic, pass transistor dual-value logic and static CMOS. Two novel topologies are presented for the 2-4 decoder: a 14-transistor topology aiming on minimizing transistor count and power dissipation and a 15-transistor topology aiming on high power-delay performance. Both a normal and an inverting decoder are implemented in each case, yielding a total of four new designs. Furthermore, four new 4-16 decoders are designed, by using mixed-logic 2-4 predecoders combined with standard CMOS post-decoder. All proposed decoders have full swinging capability and reduced transistor count compared to their conventional CMOS counterparts. Finally, a variety of comparative spice simulations at the 32 nm shows that the proposed circuits present a significant improvement in power and delay, outperforming CMOS in almost all cases.**

***Index Terms*—line decoder, mixed-logic, power-delay optimization**

I. Introduction

Static CMOS circuits are used for the vast majority of logic gates in integrated circuits [1]. They consist of complementary nMOS pulldown and pMOS pullup networks and present good performance as well as resistance to noise and device variation. Therefore, CMOS logic is characterized by robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and small transistor sizes [2]. Input signals are connected to transistor gates only, offering reduced design complexity and facilitation of cell-based logic synthesis and design.

Pass-transistor logic was mainly developed in the 1990s, when various design styles were introduced [3-6], aiming to provide a viable alternative to CMOS logic and improve speed, power and area. Its main design difference is that inputs are applied to both the gates and the source/drain diffusion terminals of transistors. Pass transistor circuits are implemented with either individual nMOS/pMOS pass transistors or parallel pairs of nMOS and pMOS called transmission gates.

This work develops a mixed-logic design methodology for line decoders, combining gates of different logic to the same circuit, in an effort to obtain improved performance compared to single-style design. Line decoders are fundamental circuits, widely used in the peripheral circuitry of memory arrays (e.g. SRAM), multiplexing structures, implementation of boolean logic functions and other applications. Despite their importance, a relatively small amount of literature is dedicated to their optimization, with some recent work including [7-9].

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The rest of this paper is organized as follows: Section II provides a brief overview of the examined decoder circuits, including logic characterization and implementation with conventional CMOS circuitry. Section III introduces and describes the new mixed-logic designs. Section IV conducts a comparative study among the proposed and conventional decoders through proper simulation, with a detailed discussion on the derived results. Section V provides the summary and final conclusions of the work presented.

II. Overview Of Line Decoder Circuits

In digital systems, discrete quantities of information are represented by binary codes. An n-bit binary code can represent up to 2^n distinct elements of coded data. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines or fewer, if the n-bit coded information has unused combinations. The circuits examined in this work are called n-to-m line decoders, and their purpose is to generate the $m = 2^n$ minterms of n input variables.

A. 2-4 Line Decoder

A 2-4 line decoder generates the 4 minterms $D_{0\text{-}3}$ of 2 input variables A and B. Its logic operation is summarized in Table I. Depending on the input combination, one of the 4 outputs is selected and set to 1 while the others are set to 0. An inverting 2-4 decoder generates the complementary minterms $I_{0\text{-}3}$, thus the selected output is set to 0 and the rest are set to 1, as shown in Table II.

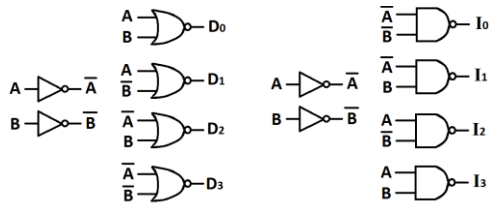
TABLE I
TRUTH TABLE OF 2-4 DECODER

A	B	D_0	D_1	D_2	D_3
0	0	**1**	0	0	0
0	1	0	**1**	0	0
1	0	0	0	**1**	0
1	1	0	0	0	**1**

TABLE II
TRUTH TABLE OF INV. 2-4 DECODER

A	B	I_0	I_1	I_2	I_3
0	0	**0**	1	1	1
0	1	1	**0**	1	1
1	0	1	1	**0**	1
1	1	1	1	1	**0**

In conventional CMOS design, NAND and NOR gates are preferred to AND and OR, since they can be implemented with 4 transistors, as opposed to 6, therefore implementing logic functions with higher efficiency. A 2-4 decoder can be implemented with 20 transistors using 2 inverters and 4 NOR gates, as shown in Fig. 1(a). The corresponding inverting



(a) (b)

Fig. 1. 20-transistor 2-4 line decoders implemented with CMOS logic: (a) Non-inverting NOR-based decoder, (b) Inverting NAND-based decoder.

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decoder can also be implemented with 20 transistors using 2 inverters and 4 NAND gates, as shown in Fig. 1(b).

B. 4-16 Line Decoder with 2-4 Predecoders

A 4-16 line decoder generates the 16 minterms $D_{0\text{-}15}$ of 4 input variables A, B, C and D, and an inverting 4-16 line decoder generates the complementary minterms $I_{0\text{-}15}$. A straightforward implementation of these circuits would require 16 4-input NOR and NAND gates. However, a more efficient design can be obtained using a predecoding technique, according to which blocks of n address bits can be predecoded into 1-of-2^n predecoded lines that serve as inputs to the final stage decoder [1]. With this technique, a 4-16 decoder can be implemented with 2 2-4 inverting decoders and 16 2-input NOR gates (Fig. 2(a)) and an inverting one can be

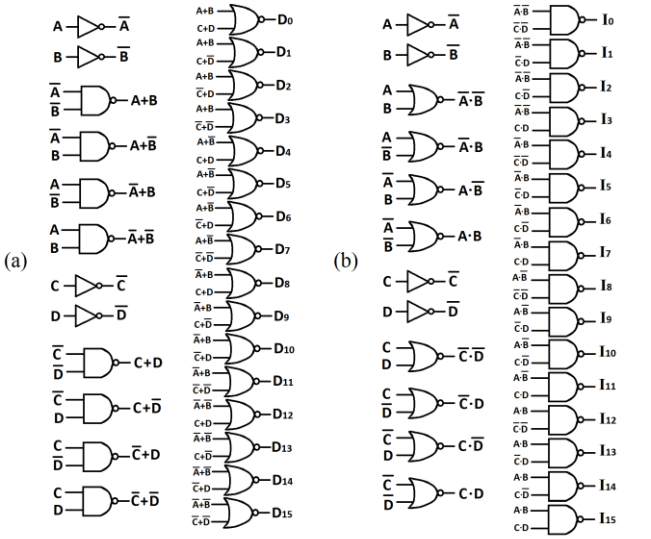

Fig. 2. 104-transistor 4-16 line decoders implemented with CMOS logic and predecoding: (a) Non-inverting decoder implemented with two 2-4 inverting predecoders and a NOR-based post-decoder, (b) Inverting decoder implemented with two 2-4 non-inverting predecoders and a NAND-based post-decoder.

implemented with 2 2-4 decoders and 16 2-input NAND gates (Fig. 2(b)). In CMOS logic, these designs require 8 inverters and 24 4-input gates, yielding a total of 104 transistors each.

III. New Mixed-Logic Designs

In combinational logic, transmission gates have mostly been used in XOR-based circuits such as full adders and as the basic switch element in multiplexers. However, we consider their use in the implementation of AND/OR logic, as demonstrated in [5], which can be efficiently applied in line decoders. The 2-input TGL AND/OR gates are shown in Fig. 3(a) and 3(b), respectively. They are full-swinging, but not restoring for all input combinations.

Regarding pass-transistor logic, there are two main circuit styles: those that use nMOS only pass-transistor circuits, like CPL [3] and those that use both nMOS and pMOS pass-transistors, like DPL [4] and DVL [6]. The style we consider in this work is DVL, which offers an improvement on DPL, preserving its full swing operation with reduced transistor count [10]. The 2-input DVL AND/OR gates are shown in Fig. 3(c) and 3(d), respectively. Similar to the TGL gates, they are full-swinging but non-restoring.

Assuming that complementary inputs are available, the TGL/DVL gates require only 3 transistors, as opposed to the 4 required in CMOS NAND/NOR gates. Decoders are high fan-

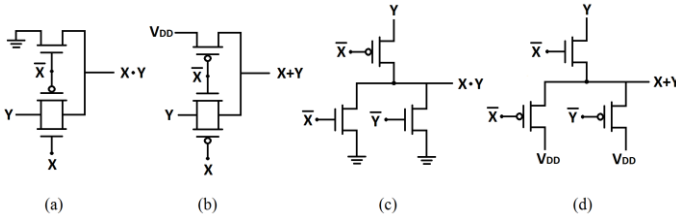

Fig. 3. The 3-transistor AND/OR gates considered in this work (a) TGL AND gate, (b) TGL OR gate, (c) DVL AND gate, (d) DVL OR gate.

out circuits, where few inverters can be used by multiple gates, thus using the TGL/DVL gates can result to reduced transistor count.

An important common characteristic of these gates is their asymmetric nature, ie the fact that they do not have balanced input loads. As shown in Fig. 3, we labeled the 2 gate inputs X and Y. In TGL gates, input X controls the gate terminals of all 3 transistors, while input Y propagates to the output node through the transmission gate. In DVL gates, input X controls 2 transistor gate terminals, while input Y controls 1 gate terminal and propagates through a pass transistor to the output. We will refer to X and Y inputs as the control signal and the propagate signal of the gate, respectively.

This asymmetric feature gives a designer the flexibility to perform signal arrangement, ie choosing which input is used as control and which as propagate signal in each gate. Having a complementary input as propagate signal is not a good practice, since the inverter added to the propagation path increases delay significantly. Therefore, when implementing the inhibition (A'B) or implication (A'+B) function, it is more efficient to choose the inverted variable as control signal. When implementing the AND (AB) or OR (A+B) function, either choice is equally efficient. Finally, when implementing the NAND (A'+B') or NOR (A'B') function, either choice results to a complementary propagate signal, perforce.

A. The 14-transistor 2-4 Low-Power Topology

Designing a 2-4 line decoder with either TGL or DVL gates would require a total of 16 transistors (12 for AND/OR gates and 4 for inverters). However, by mixing both AND gate types into the same topology and using proper signal arrangement, it is possible to eliminate one of the two inverters, therefore reducing the total transistor count to 14.

Let us assume that, out of the two inputs, namely A and B, we aim to eliminate the B inverter from the circuit. The D_o minterm (A'B') is implemented with a DVL gate, where A is used as propagate signal. The D_1 minterm (AB') is implemented with a TGL gate, where B is used as propagate signal. The D2 minterm (A'B) is implemented with a DVL gate, where A is used as propagate signal. Finally, The D_3 minterm (AB) is implemented with a TGL gate, where B is used as propagate signal. These particular choices completely avert the use of the complementary B signal, therefore the B

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inverter can be eliminated from the circuit resulting in a 14-transistor topology (9 nMOS, 5 pMOS).

Following a similar procedure with OR gates, a 2-4 inverting line decoder can be implemented with 14 transistors (5 nMOS, 9 pMOS), as well: I_0, I_2 are implemented with TGL (using B as propagate signal) and I_1, I_3 are implemented with DVL (using A as propagate signal). The B inverter can once again be elided.

The inverter elimination reduces transistor count, logical effort and overall switching activity of the circuits, thereby minimizing power dissipation. As far as the authors are concerned, 14 is the minimum number of transistors required to realize a full-swinging 2-4 line decoder with static (non-clocked) logic. The two new topologies are named '2-4LP' and '2-4LPI', where 'LP' stands for 'low power' and 'I' for 'inverting'. Their schematics are shown in Fig. 4(a) and Fig. 4(b), respectively.

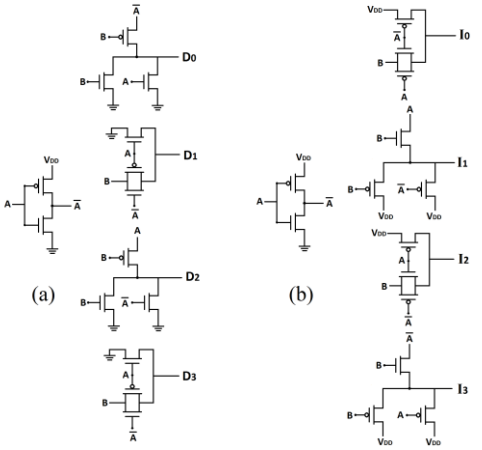

Fig. 4. New 14-transistor 2-4 line decoders: (a) 2-4LP (b) 2-4LPI.

B. *The 15-transistor 2-4 High-Performance Topology*

The low-power topologies presented above have a drawback regarding worst case delay, which comes from the use of complementary A as the propagate signal in the case of D_0 and I_3. However, realizing D_0 and I_3 can be implemented more efficiently by using standard CMOS gates, since there is no need for complementary signals. Specifically, D_0 can be implemented with a CMOS NOR gate and I_3 with a CMOS NAND gate, adding one transistor to each topology. The new designs resulting from this modification mix 3 different types of logic into the same circuit and present a significant improvement in delay while only slightly increasing power dissipation. They are named '2-4HP' (9 nMOS, 6 pMOS) and '2-4HPI' (6 nMOS, 9 pMOS), where 'HP' stands for 'high performance' and 'I' for 'inverting'. The reasoning behind the 'HP' designation is that these decoders present both low power and low delay characteristics, therefore achieving an overall good performance. The 2-4HP and 2-4HPI schematics are shown in Fig. 5(a) and Fig. 5(b), respectively, where the additional transistors are highlighted for easier distinction.

C. *Integration in 4-16 Line Decoders*

At a small scale, circuits based on pass transistor logic can realize logic functions with fewer transistors and improved performance compared to static CMOS. However, cascading several non-restoring circuits causes a rapid degradation in performance. A mixed-topology approach, ie alternating restoring and non-restoring levels of logic, can potentially deliver optimum results, combining the positive characterists of both.

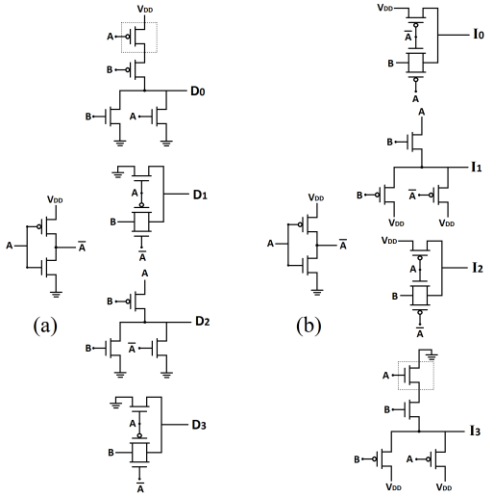

Fig. 5. New 15-transistor 2-4 line decoders: (a) 2-4HP (b) 2-4HPI.

Adopting this design methodology, and with respect to the theory presented on section II, we implemented four 4-16 decoders by using the four new 2-4 as predecoders in conjunction with CMOS NOR/NAND gates to produce the decoded outputs. The new topologies derived from this combination are: 4-16LP (Fig. 6(a)), which combines two 2-4LPI predecoders with a NOR-based post-decoder, 4-16HP (Fig. 6(b)), which combines two 2-4HPI predecoders with a NOR-based post-decoder, 4-16LPI (Fig. 6(c)), which combines two 2-4LP predecoders with a NAND-based post-decoder and, finally, 4-16HPI (Fig. 6(d)), which combines two 2-4HP predecoders with a NAND-based post-decoder.

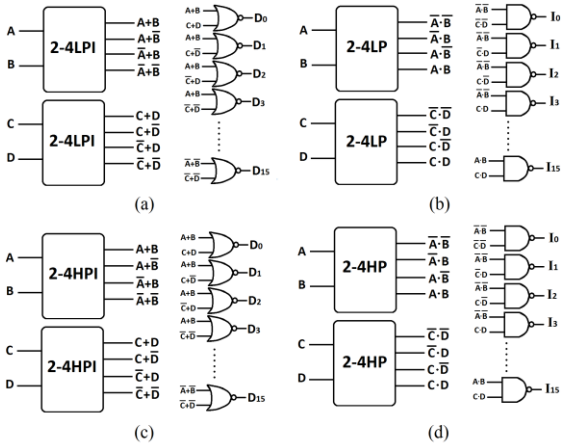

Fig. 6. New 4-16 line decoders: (a) 4-16LP, (b) 4-16LPI, (c) 4-16HP, (d) 4-16HPI.

The 'LP' topologies have a total of 92 transistors, while the 'HP' ones have 94, as opposed to the 104 transistors required by the pure CMOS implementation.

IV. Simulations

In this section, we perform a variety of BSIM4-based spice simulations on the schematic level, in order to compare the proposed mixed-logic decoders with the conventional CMOS. All the examined circuits are implemented using a 32 nm

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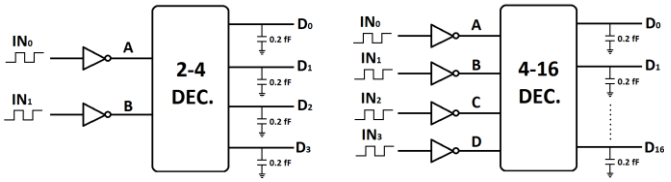
predictive technology model for low-power applications (PTM LP), incorporating high-k/metal gate and stress effect [11]. Since our main focus is low-power design, we use unit-size transistors exclusively (L_n=L_p= 32 nm, W_n=W_p= 64 nm) for all decoders.

A. Simulation Setup

All circuits are simulated under 3 different operating frequencies (0.5, 1.0 and 2.0 GHz) and 3 different supply/input voltages (0.8, 1.0 and 1.2 V), for a total of 9 simulations. Each one of these simulations is repeated 5 times with varying temperature (-50, -25, 0, 25 and 50 C^o) and the average power/delay is calculated and presented in each case. All inputs are buffered with inverters and all outputs are loaded with an output capacitance of 0.2 fF, as shown in Fig. 7. The input inverters have a W_p/W_n ratio of 2 (L_n=L_p= 32 nm, W_n= 64 nm, W_p= 128 nm), in order to offer an overall balanced switching performance.

Furthermore, proper bit sequences are inserted to the inputs



(a) (b)

Fig. 7. Simulation setup regarding input/output loading conditions: (a) 2-4 decoders, (b) 4-16 decoders.

in the form of rectangular pulses, in order to cover all possible transitions a decoder can perform. A 2-4 decoder has 2 inputs, which can generate 2^2=4 different binary combinations, thus yielding a total of 4*4=16 possible transitions (we include the transitions from and to the same combination). The 2-4 decoders are simulated for 64 nanoseconds (ns), so that the 16-bit input sequences are repeated 4 times. Similarly, a 4-16 decoder has 4 inputs, 4^2=16 input combinations and 16*16=256 possible transitions, therefore the 4-16 decoders are simulated for 256 ns to exactly cover all transitions once. Fig. 8 depicts the input/output waveforms of our proposed 2-4 decoders for all 16 input transitions, showing their full swinging capability despite using pass-transistor gates.

B. Performance Metrics Examined

The metrics considered for the comparison are: average power dissipation, worst-case propagation delay and power-delay product.

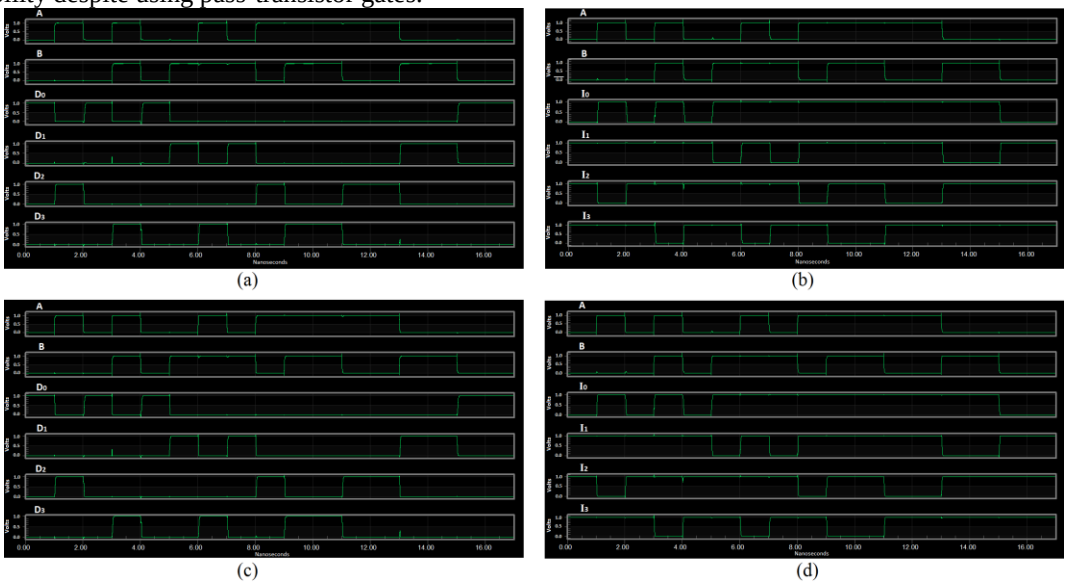
With continuous sub-micron scaling, especially at low voltage operation, leakage power consumption has become increasingly important as it dominates the dynamic one [12]. In our analysis, both leakage and active currents are considered. The total power dissipation (static+dynamic) is extracted from spice simulation and given in nanowatts (nW). Regarding the delay, we note the highest value that occurs among all transitions and outputs in each case, given in picoseconds (ps). The power-delay product (PDP) measures the energy per operation/switching event. It is calculated as average *power*max delay* and given in electronvolts (eV).

C. Results Discussion

The simulation results regarding power, PDP and delay are shown in Table III, Table IV and Table V, respectively. Table V does not include varied frequency, since propagation delay is independent of that parameter. With respect to the results, each of the proposed designs will be compared to its conventional CMOS counterpart, considering the average simulation measurements in each case. Specifically, 2-4LP, 2-4HP are compared to 20T, 2-4LPI, 2-4HPI are compared to inverting 20T, 4-16LP, 4-16HP are compared to 104T and 4-16LPI, 4-16HPI are compared to inverting 104T.

According to the obtained results, 2-4LP presents 9.3% less power dissipation than CMOS 20T. Other than that, it comes of to be a slow topology, introducing a cost of 26.7% higher delay and 15.7% higher PDP. On the other hand, 2-4HP outperforms CMOS 20T in all aspects, reducing power, delay, and PDP by 8.2%, 4.3% and 15.7%, respectively. Both of our inverting designs, 2-4LPI and 2-4HPI, outperform CMOS 20T inv. in all aspects, as well. Specifically, 2-4LPI reduces power, delay and PDP by 13.3%, 11%, and 25%, respectively, while 2-4HPI does so by 11.2%, 13.2% and 25.7%.

Regarding the 4-16 simulations, the obtained results are similar. The 4-16LPI decoder, which uses the slower 2-4LP as



(a) (b)

(c) (d)

Fig. 8. Input/Output waveforms of proposed 2-4 decoders for all input transitions: (a) 2-4LP, (b) 2-4LPI, (c) 2-4HP, (d) 2-4HPI.

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TABLE III
POWER DISSIPATION RESULTS (NW)

2-4 DEC.	500 MHZ			1 GHZ			2 GHZ			4-16 DEC.	500 MHZ			1 GHZ			2 GHZ		
	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V		0.8V	1.0V	1.2V	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V
CMOS	269	415	622	545	862	1287	1100	1768	2636	**CMOS**	841	1349	2030	1692	2751	4112	3393	5564	8310
2-4LP	246	386	576	495	790	1173.1	996	1594	2369	**4-16LP**	785	1258	1878	1577	2546	3816	3160	5140	7662
2-4HP	248	391	583	499	800	1185	1004	1618	2397	**4-16HP**	791	1270	1905	1588	2572	3847	3182	5198	7749
CMOS INV.	268	421	631	849	867	1290	1095	1767	2622	**CMOS INV.**	843	1330	2000	1698	2735	4096	3412	5562	8327
2-4LPI	242	381	567	488	778	1155	984	1571	2337	**4-16LPI**	788	1265	1888	1584	2566	3827	3178	5179	7724
2-4HPI	245	389	578	495	793	1175	998	1604	2377	**4-16HPI**	793	1271	1894	1592	2580	3841	3194	5209	7758

TABLE IV
POWER-DELAY-PRODUCT RESULTS (EV)

2-4 DEC.	500 MHZ			1 GHZ			2 GHZ			4-16 DEC.	500 MHZ			1 GHZ			2 GHZ		
	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V		0.8V	1.0V	1.2V	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V
CMOS	176	127	128	357	264	265	720	541	543	**CMOS**	1123	817	836	2260	1666	1694	4532	3369	3423
2-4LP	203	149	155	408	306	315	821	617	636	**4-16LP**	995	730	750	1998	1478	1524	4004	2984	3061
2-4HP	153	115	120	308	235	244	620	475	494	**4-16HP**	963	698	702	1933	1413	1417	3873	2855	2854
CMOS INV	167	126	134	530	260	274	683	529	556	**CMOS INV.**	1326	897	886	2671	1844	1815	5367	3749	3690
2-4LPI	134	102	106	271	209	216	547	422	438	**4-16LPI**	1328	940	931	2669	1906	1887	5356	3846	3809
2-4HPI	133	102	105	269	208	213	542	420	430	**4-16HPI**	1203	849	839	2415	1723	1702	4844	3479	3438

TABLE V
PROPAGATION DELAY RESULTS (PS)

2-4 DEC.	0.8V	1.0V	1.2V	4-16 DEC.	0.8V	1.0V	1.2V
CMOS	105	49	33	**CMOS**	214	97	66
2-4LP	132	62	43	**4-16LP**	203	93	64
2-4HP	99	47	33	**4-16HP**	195	88	59
CMOS INV	100	48	34	**CMOS INV.**	252	108	71
2-4LPI	89	43	30	**4-16LPI**	270	119	79
2-4HPI	87	42	29	**4-16HPI**	243	107	71

predecoder, presents 6.4% lower power dissipation with the cost of 17.9% higher delay and 1.9% higher PDP than CMOS 104T. The rest of the decoders, namely 4-16LP, 4-16HP and 4-16HPI, present better results than corresponding CMOS decoders in all cases, which can be summarized as: 7.4%, 6.5% and 6.0% lower power, 4.5%, 9.3% and 2.3% lower delay and 11.1%, 15.3% and 7.9% lower PDP, respectively.

V. CONCLUSIONS

This paper introduced an efficient mixed-logic design for decoder circuits, combining TGL, DVL and static CMOS. By using this methodology, we developed four new 2-4 line decoder topologies, namely 2-4LP, 2-4LPI, 2-4HP and 2-4HPI, which offer reduced transistor count (therefore potentially smaller layout area) and improved power-delay performance in relation to conventional CMOS decoders.

Furthermore, four new 4-16 line decoder topologies were presented, namely 4-16LP, 4-16LPI, 4-16HP and 4-16HPI, realized by using the mixed-logic 2-4 decoders as predecoding circuits and combining them with post-decoders implemented in static CMOS logic. These designs combine the improved performance characteristics of pass transistor logic with the restoring capability of static CMOS.

A variety of comparative spice simulations was performed at the 32 nm, verifying, in most cases, a definite advantage in favor of the proposed designs. The 2-4LP and 4-16LPI topologies are mostly suitable for applications where area and power minimization is of primary concern. The 2-4LPI, 2-4HP and 2-4HPI, as well as the corresponding 4-16 topologies (4-16LP, 4-16HPI, 4-16HP), proved to be viable and all-around efficient designs, thus they can effectively be used as building blocks in the design of larger decoders, multiplexers and other combinational circuits of varying performance requirements.

Moreover, the presented reduced transistor count and low power characteristics can benefit both bulk CMOS and SOI design as well. The obtained circuits are to be implemented on layout level, making them suitable for standard cell libraries and RTL design.

REFERENCES

[1] N. H. E. Weste and D. M. Harris, "*CMOS VLSI Design, a Circuits and Systems Perspective*," 4th ed., 2011: Addison-Wesley.

[2] R. Zimmermann and W. Fichtner, "Low-Power Logic Styles: CMOS Versus Pass-Transistor Logic", *IEEE Journal of Solid State Circuits*, vol. 32, no. 7, pp.1079 -1090, 1997.

[3] K. Yano, et al., "A 3.8-ns CMOS 16x16-b multiplier using complementary pass-transistor logic," *IEEE J. Solid-State Circuits*, vol. 25, pp.388 -393, 1990.

[4] M. Suzuki, et al., "A 1.5ns 32b CMOS ALU in double pass-transistor logic," *Proc. 1993 IEEE Int. Solid-State Circuits Conf.*, pp.90 -91 1993.

[5] X. Wu, "Theory of transmission switches and its application to design of CMOS digital circuits," *International J. Circuit Theory and Application*, vol. 20, no. 4, pp.349 -356, 1992.

[6] V. G. Oklobdzija and B. Duchene, "Pass-transistor dual value logic for low-power CMOS," *Proc. of the Int. Symp. on VLSI Technology*, pp.341 -344 1995.

[7] M. A. Turi and J.G. Delgado-Frias, "Decreasing energy consumption in address decoders by means of selective precharge schemes," *Microelectronics Journal*, vol. 40, no. 11, pp.1590-1600, 2009.

[8] V. Bhatnagar, A. Chandani and S. Pandey, "Optimization of row decoder for 128×128 6T SRAMs," *2015 International Conference on VLSI Systems, Architecture, Technology and Applications (VLSI-SATA)*, pp. 1-4. IEEE, 2015.

[9] A. K. Mishra, D. P. Acharya and P. K. Patra, "Novel design technique of address Decoder for SRAM," *2014 International Conference on Advanced Communication Control and Computing Technologies (ICACCCT)*, pp. 1032-1035, IEEE, 2014.

[10] D. Marković, B. Nikolić and V.G. Oklobdžija, "A general method in synthesis of pass-transistor circuits," *Microelectronics Journal*, vol 31, pp. 991-998, 2000.

[11] Available at: http://ptm.asu.edu/

[12] N. Lotze and Y. Manoli, "A 62 mV 0.13 µm CMOS Standard-Cell-Based Design Technique Using Schmitt-Trigger Logic," *IEEE Journal of Solid State Circuits*, vol. 47, no.1, pp. 47-60, Jan. 2012.