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A High-Voltage-Gain DC-DC Converter Based on Modified Dickson Charge Pump Voltage Multiplier

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***Abstract* - A high-voltage-gain dc-dc converter is introduced in this paper. The proposed converter resembles a two-phase interleaved boost converter on its input side while having a Dickson charge pump based voltage multiplier on its output side. This converter offers continuous input current which makes it more appealing for the integration of renewable sources like solar panels to a 400-V dc bus. Also, the proposed converter is capable of drawing power from either a single source or two independent sources. Furthermore, the voltage multiplier used offers low voltage ratings for capacitors which potentially leads to size reduction. The converter design and component selection has been discussed in detail with supporting simulation results. A hardware prototype of the proposed converter with V_{in}=20V and V_{out}=400V has been developed to validate the analytical results.**

***Index Terms* - Voltage multiplier, modified Dickson charge pump, high-voltage-gain dc-dc power electronic converter**

I. INTRODUCTION

Distribution systems at 400-V dc have been gaining popularity as they offer better efficiency, higher reliability at an improved power quality, and low cost compared to ac distribution systems [1-4]. They offer a simpler integration of renewable energy and energy storage systems. Currently, telecom centers, data centers, commercial buildings, residential buildings, and microgrids are among the emerging examples of dc distribution systems [5-7]. One of the challenges facing such systems is the power electronic converters for integrating renewable sources into the 400-V dc bus. A typical voltage range for solar panels is between 20V dc to 40V dc. Stepping up these voltages to 400-V dc using classic boost and buck-boost converters requires high duty ratios which results in high component stress and lower efficiency. Therefore, a typical choice would be using two cascaded converters; which results in inefficient operation, reduced reliability, increased size, and stability issues. Isolated topologies like flyback, forward, half-bridge, full-bridge, and push-pull converters have discontinuous input currents and hence would require large input capacitors.

High-voltage-gain dc-dc converters using a boost stage followed by voltage multiplier (VM) cells have been proposed in [8-11]. Table I summarizes these converters based on their individual component count, voltage gain, and voltage stress on their switches. The second order hybrid boosting converter proposed in [8] offers relatively low voltage gain in comparison to its voltage multiplier component count. It also has a very large input current ripple in proportion to its average. High step-up converters using single-inductor-energy-storage-cell-based switched capacitors proposed in [9] do not offer voltage gains high enough to boost a 20V input to 400V at an reasonable switching duty cycle. The multiple-inductor-energy-storage-cell-based switched capacitor based high voltage converters [9] offer a relatively low voltage gain in proportion to its component count. The switched-capacitor-based active-network converter proposed in [10] has a discontinuous input current ripple due to the series and parallel connection of the inductors in its two modes of operation. The transformer-less high-gain boost converter proposed in [11] offers continuous input current but the switches experience a high voltage stress – more than 2/3rd of its output voltage.

TABLE I
HIGH-VOLTAGE-GAIN CONVERTERS USING BOOST STAGE AND VOLTAGE MULTIPLIER CIRCUITS

Topology	[8]	[9]	[10]	[11]
No. of switches	1	1	2	2
No. of inductors	1	1	2	2
No. of capacitors	4	3	3	3
No. of diodes	4	3	3	4
V_{out}/V_{in}	$\frac{3-d}{1-d}$	$\frac{2}{1-d}$	$\frac{3+d}{1-d}$	$\frac{1}{d(1-d)}$
V_{Switch}/V_{out}	$\frac{1}{3-d}$	$\frac{1}{2}$	$\frac{1}{3+d}$	$(1-d), d$
Input current	Discontinuous	Continuous	Discontinuous	Continuous

High-voltage-gain dc-dc converters using coupled inductors and high frequency transformers have been proposed for the integration of solar panels to 400V dc bus [12-18]. In such converters, the design of high frequency transformers and coupled inductors is complicated as the leakage inductance increases when higher voltage gains are intended. As a result, the converter switches experience large voltage spikes and therefore would require clamping circuitry to reduce the voltage stress on the switches. These clamping circuits have a negative effect on the converter voltage gains. A family of non-isolated high-voltage-gain dc-dc converters

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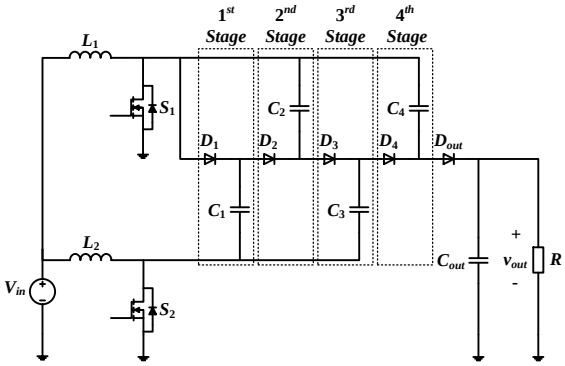
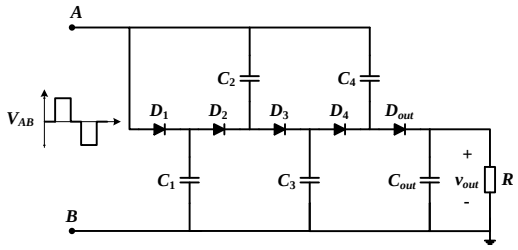
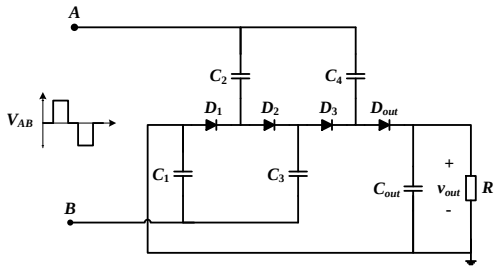


Fig. 1. High-voltage-gain dc-dc converter proposed in [19]



(a) Dickson charge pump



(b) Modified Dickson charge pump

Fig. 2. Conventional and modified Dickson charge pump voltage multiplier circuits

that makes use of VM cells derived from the Dickson charge pump (see Fig. 1) has been proposed in [19]. The voltage rating of each VM cell capacitor is twice that of its previous VM cell. Also, the inductors (L_1, L_2) and switches (S_1, S_2) experience different current stresses whenever even number of VM cells is used.

A high-voltage-gain dc-dc converter based on the modified Dickson charge pump voltage multiplier circuit is introduced in this paper. This converter is capable of stepping up voltages as low as 20V to 400V. The proposed converter offers continuous input current and low voltage stress ($1/4^{th}$ of its output voltage) on its switches. This converter can draw power from a single source or two independent sources while having continuous input currents, which makes it suitable for applications like solar panels. Compared to the topology presented in [19], the proposed converter requires lower voltage rating capacitors for its VM circuit and also one less diode. The inductors and switches experience identical current stresses making the component selection process for the converter simpler.

In section II, the modified Dickson charge pump voltage multiplier circuit has been discussed. Section III introduces modes of operations. The voltage gain of the proposed converter has been derived in section IV. Section V analyzes the component stress and provides supporting simulation results. Section VI discusses the experimental results obtained using the hardware prototype. A comparative analysis of the proposed converter and the high-voltage-gain converter shown in Fig. 1 has been discussed in section VII. Finally, section VIII concludes the paper.

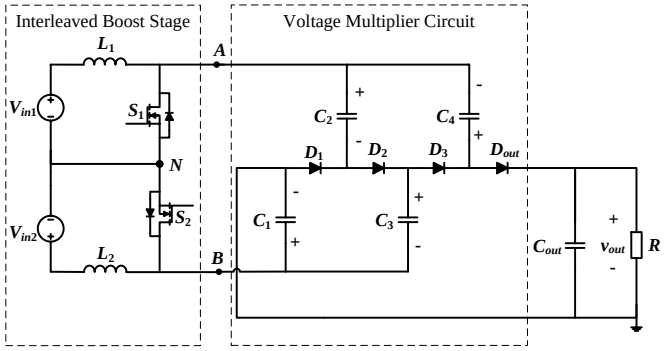


Fig. 3. Proposed high-voltage-gain dc-dc converter

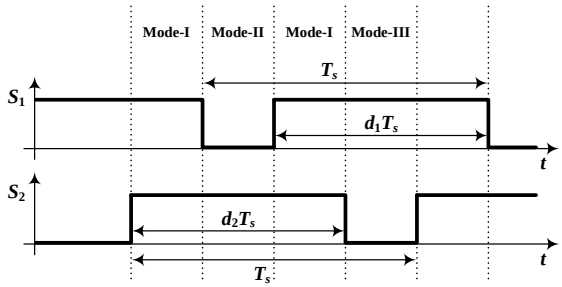


Fig. 4. Input boost converter switching signals for the proposed converter

II. Modified Dickson Charge Pump Voltage Multiplier

The Dickson charge pump voltage multiplier circuit [20] shown in Fig. 2a offers a boosted dc output voltage by charging and discharging its capacitors. The input voltage (V_{AB}) is a modified square wave (MSW) voltage. The voltages of the capacitors in the Dickson charge pump double at each stage as one traverses from the input side capacitor C_1 to the load side capacitor C_4. For an output voltage of V_{out} = 400V, the voltages of capacitors C_1, C_2, C_3, and C_4 are 80V, 160V, 240V, and 320V respectively.

The authors propose to make a slight modification to the Dickson charge pump circuit as shown in Fig. 2b. For a same output voltage, the voltages of all the capacitors in the modified Dickson charge pump are smaller than the voltage of capacitor C_2 in the Dickson charge pump. For an output voltage of V_{out} = 400V, the voltages of capacitors C_1, C_2, C_3, and C_4 are only 150V, 50V, 50V, and 150V, respectively Therefore the volume of the capacitors used in the proposed modified Dickson charge pump voltage multiplier circuit is potentially less compared to the Dickson charge pump.

III. Topology and Modes of Operation

The proposed converter provides a high voltage gain using the modified Dickson charge pump voltage multiplier circuit (see Fig. 3). On a closer look, it can be seen that the converter

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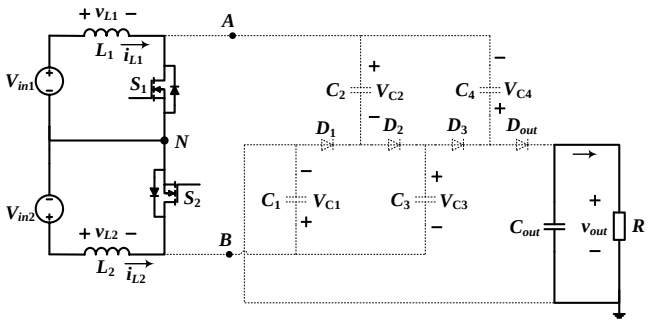

Fig. 5. Proposed converter operation in mode-I

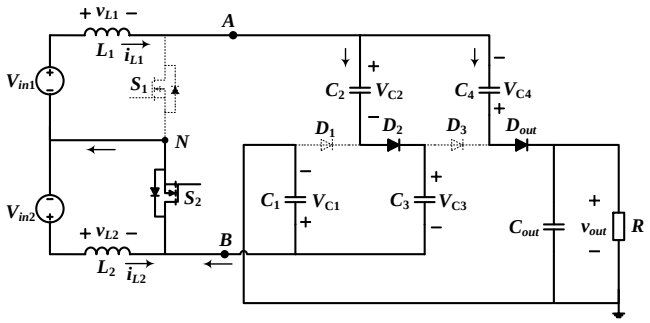

Fig. 6. Proposed converter operation in mode-II

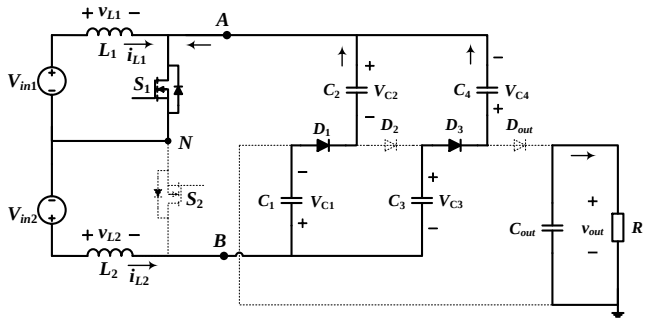

Fig. 7. Proposed converter operation in mode-III

is made up of two stages. The first stage is a two-phase interleaved boost converter which outputs an MSW voltage between its output terminals *A* and *B*. The second stage is the modified Dickson chare pump voltage multiplier circuit that boosts the MSW voltage (V_{AB}) to provide a higher dc output voltage. The gating signals of the two interleaved boost stage switches S_1 and S_2 are shown in Fig. 4. For the proposed converter to operate normally, both switches S_1 and S_2 must have an overlap time where both are ON and also one of the switches must be ON at any point of time. This can be achieved by using duty ratios of greater than 50% for both the switches and having them operate at 180 degrees out of phase from each other. As can be seen from Fig. 4, such gate signals lead to three different modes of operation which are explained as follows.

A. Mode I

In this mode, both switches S_1 and S_2 of the two-phase interleaved boost converter are ON (see Fig. 5). Input sources V_{in1} and V_{in2} charge inductors L_1 and L_2 respectively. Inductor currents i_{L1} and i_{L2} both increase linearly. All the diodes of the voltage multiplier circuit are reverse-biased and hence OFF. The voltages of the multiplier capacitors remain same and the output diode D_{out} is reverse biased. Therefore, the load is supplied by the output capacitor.

B. Mode II

In this mode, switch S_1 is OFF and switch S_2 is ON. Diodes D_1 and D_3 are OFF as they are reverse biased while diodes D_2 and D_{out} are ON as they are forward biased (see Fig. 6). A part of inductor current i_{L1} flows through capacitors C_2 and C_3 and thereby charging them. The remaining current flows through the capacitors C_4 and C_1 discharging them to charge the output capacitor C_{out} and supply the load.

C. Mode III

In this mode switch S_1 is ON and switch S_2 is OFF (see Fig. 7). Diodes D_1 and D_3 are ON as they are forward biased while diodes D_2 and D_{out} are OFF as they are reverse biased. Inductor current i_{L2} flows through diode-capacitor voltage multiplier cell capacitors C_1, C_2, C_3, and C_4. Capacitors C_1 and C_4 are charged while discharging capacitors C_2 and C_3. In this mode, the output capacitor supplies the load.

IV. Voltage Gain of the Converter

In the proposed converter, the input power is transferred to the output by charging and discharging the voltage multiplier circuit capacitors. For an ideal converter shown in Fig. 3, the voltage gain of the converter can be derived as described below. For inductors L_1 and L_2, the average voltage across the inductors according to volt-second balance can be written as

$$\langle V_{L1}\rangle = \langle V_{L2}\rangle = 0 \tag{1}$$

From Fig. 6, based on the volt-second balance of inductor L_1, one can write

$$V_{AN} = V_{C2} + V_{C3} = V_{out} - V_{C1} - V_{C4} = \frac{V_{in1}}{(1-d_1)} \tag{2}$$

where d_1 is the duty cycle of switch S_1. From Fig. 7, based on the volt-second balance of the inductor L_2, one can write

$$V_{BN} = V_{C1} - V_{C2} = V_{C4} - V_{C3} = \frac{V_{in2}}{(1-d_2)} \tag{3}$$

Assuming capacitors C_2 and C_3 are identical, the voltage across them would be equal and can be written as

$$V_{C2} = V_{C3} = \frac{1}{2} \times \frac{V_{in1}}{(1-d_1)} \tag{4}$$

By substituting (4) in (3), one can derive capacitor voltages V_{C1} and V_{C4} to be

$$V_{C1} = V_{C4} = \frac{1}{2} \times \frac{V_{in1}}{(1-d_1)} + \frac{V_{in2}}{(1-d_2)} \tag{5}$$

Finally, the output voltage is derived by substituting (5) in (2) which yields

$$V_{out} = \frac{2 \times V_{in1}}{(1-d_1)} + \frac{2 \times V_{in2}}{(1-d_2)} \tag{6}$$

The proposed converter can be supplied from two inputs (see Fig. 3) as well as using only one input source. When a single input is used for the proposed converter, switches S_1 and S_2 have the same switching duty cycle '*d*' and are 180 degrees out of phase from each other. The proposed converter with single source is shown in Fig. 8. The multiplier circuit capacitor voltages and the output voltage are simplified as shown below.

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$$V_{C2} = V_{C3} = \frac{1}{2} \times \frac{V_{in}}{(1-d)} \quad (7)$$

$$V_{C1} = V_{C4} = \frac{3}{2} \times \frac{V_{in}}{(1-d\ )} \quad (8)$$

$$V_{out} = \frac{4 \times V_{in}}{(1-d)} \quad (9)$$

A 20-V input source at 80% switching duty cycle will generate an output voltage of 400V using the proposed converter in Fig. 8. Capacitors C_1 and C_4 are charged to 150V and capacitors C_2 and C_3 are charged to 50V.

V. Component Stress and Simulation Results

This section discusses the voltage and current stresses observed by different components and also provide simulation waveforms during steady-state operation of the proposed converter. The discussions in this section are based on the topology shown in Fig. 8, i.e., using a single voltage source to power the converter while operating both switches S_1 and S_2 of the two-phase interleaved boost stage at a fixed duty cycle d. A simulation model of the proposed converter has been built in PLECS blockset of MATLAB. The parameters used in the simulation are given in Table II.

A. Inductor

The inductor currents in both phases of the interleaved boost stages are similar. The average inductor currents can be calculated using (10). The rms value of the inductor currents used in the calculation of inductor copper losses can be calculated as shown in (11).

$$I_{L1,avg} = I_{L2,avg} = \frac{2 \times I_{out}}{(1-d)} \quad (10)$$

$$I_{L1,rms} = I_{L2,rms} = \sqrt{\left(\frac{2 \times I_{out}}{1-d}\right)^2 + \left(\frac{V_{in} \times d}{2\sqrt{3} \times L \times f_{sw}}\right)^2} \quad (11)$$

The inductance required for a current ripple of ΔI_L is given by

$$L_1 = L_2 = L = \frac{V_{in} \times d}{\Delta I_L \times f_{sw}} \quad (12)$$

From (10), (11), and (12), it is observed that both the inductors carry same amount of current and require same inductance for an assumed current ripple. Therefore, a similar inductor can be used for both L_1 and L_2. Moreover as the rms currents of inductors L_1 and L_2 are equal, minimal conduction losses can be achieved in the inductors compared to other similar converters (see Fig. 1) having different values of currents flowing through their boost stage inductors. The inductor current and voltage waveforms obtained from PLECS simulation are shown in Fig. 9. At 200W of output power, both the inductors carry a current of 5A with a ripple of 1.6A in each.

B. Input Current

The input source is connected to an interleaved two-phase boost stage. Since it is a boost converter on the input side, the input current is continuous. As the two phases of the interleaved boost are 180 degrees out of phase from each other, the input current ripple is even smaller. This greatly reduces the size of the input filter capacitor required for the converter. The input current waveform of the proposed converter operating at 200W is shown in Fig. 9. It can be seen that the ripple of the input current is about 1.2A even though inductor currents i_{L1} and i_{L2} have a ripple of 1.6A each. The reason for this smaller input current ripple is both the boost switches being operated 180 degrees out of phase from each other.

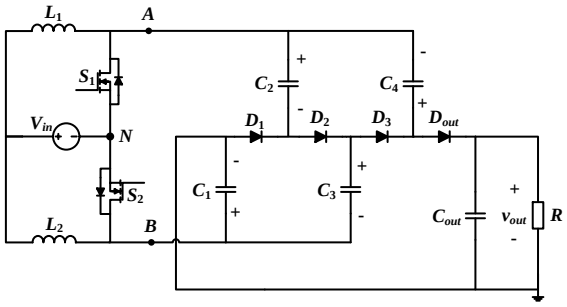

Fig. 8. Proposed converter with single input source

TABLE II
Simulation Parameters

Parameter	Value
Input Voltage	20 V
Output Voltage	400 V
Load Resistance	800 Ω
Duty cycle of switches S_1 and S_2	80%
Switching Frequency - f_{sw}	100 kHz
Boost Inductors L_1 and L_2	100 µH
VM capacitors	60 µF
Output Capacitor	22 µF

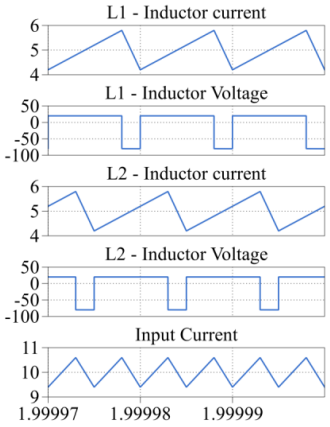

Fig. 9. Inductor L_1 and L_2 – current and voltage waveforms, Input current

C. Switches

The maximum voltage observed across the switches in the proposed converter is equal to the output of its boost stage. This is a small number compared to the high output voltage of the proposed converter. The switch blocking voltages can be calculated using (13). As current in both the inductors is the same, the current stress on both switches is same as well. The average current in the switches can be calculated using (14).

$$V_{S1} = V_{S2} = \frac{V_{in}}{(1-d)} \quad (13)$$

$$I_{S1,avg} = I_{S2,avg} = \frac{2 \times I_{out}}{(1-d)} \quad (14)$$

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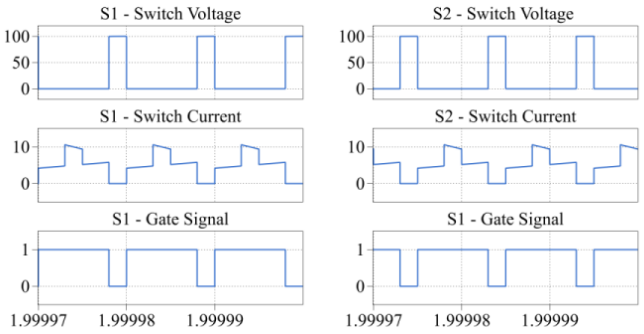
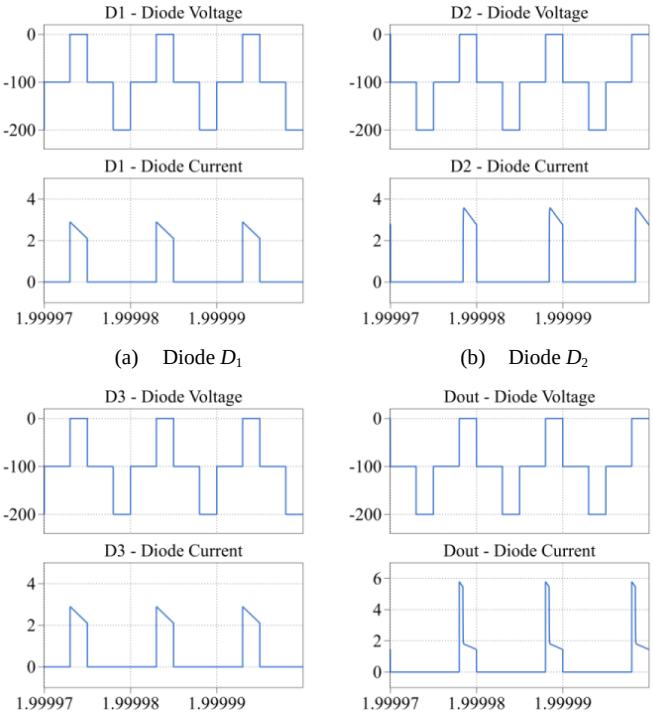


(a) Switch S_1 (b) Switch S_2

Fig. 10. Switch voltage, current and gate signal waveforms



(a) Diode D_1 (b) Diode D_2

(a) Diode D_3 (b) Output Diode D_{out}

Fig. 11. Diode voltage and current waveforms

TABLE III
COMPONENT SPECIFICATIONS OF THE HARDWARE PROTOTYPE

Component	Name	Rating	Part No
Inductor	L_1, L_2	100 µH, DCR=11 mΩ	CTX100-10-52LP
MOSFET	S_1,S_2	150 V, 43 A, Rds(on)=7.5 mΩ	IPA075N15N3G
Diode	D_1, D_2, D_3, D_{out}	250 V, 40 A, V_F=0.97 V	MBR40250T
VM capacitors	C_1, C_2, C_3, C_4	60 µF, 250 V, ESR=2.6 mΩ	C4ATDBW5600A3OJ
Output Capacitor	C_{out}	22 uF, 450 V, ESR=6.2 mΩ	B32774D4226

The waveforms of the switches in the proposed converter are shown in Figs. 10(a) and 10(b). Switches S_1 and S_2 have the same current and voltage stress as can be seen in the simulation waveforms. Since the converter in simulation is operating at 80% switching duty cycle with a 20V input, the maximum voltage stress seen on both switches is only 100V. Both switches S_1 and S_2 carry an average current of 5A.

D. Diodes

The diodes experience two times higher blocking voltages compared to the switches as it depends on the voltages of the voltage multiplier circuit capacitors. In this topology, all the diodes experience the same blocking voltage which can be calculated using (15). The average current in the diode can be calculated using (16). Since all the diodes experience same maximum voltage stress, similar diodes can be used for all of them.

$$V_{D1} = V_{D2} = V_{D3} = V_{Dout} = \frac{2 \times V_{in}}{(1-d)} \tag{15}$$

$$I_{D1,avg} = I_{D2,avg} = I_{D3,avg} = I_{Dout,avg} = I_{out} \tag{16}$$

The voltage and current waveforms of diodes D_1, D_2, D_3, and D_{out} in the proposed converter are shown in Fig. 11. For the converter operating at 80% switching duty cycle and 20V input, the maximum blocking voltage seen by the diodes is 200V. The diodes conduct either only during mode II or mode III of the converter operation. All the diodes carry an average current of 0.5A which is equal to the output current. Diodes D_2 and D_{out} have different current waveforms. This is because of the voltage imbalance in the capacitors during the start of mode II. Only diode D_{out} initially conducts in order to charge the output capacitor and bring in a balance in the voltage. Once the voltage loops are balanced, then the current flowing through the diodes is dependent on the impedance of the capacitors.

VI. EXPERIMENTAL RESULTS

A hardware prototype of the proposed converter was built to test and validate the proposed converter operation. The specifications of the components used for building the hardware prototype are given in Table III. The power rating of the converter is 400W with an input voltage of 20V and an output voltage of 400V. The proposed converter is tested at a switching frequency of 100 kHz.

A theoretical loss analysis is performed using the ratings of the selected components of the hardware prototype. The converter is assumed to operate at 200W of output power. The calculated losses include conduction losses in inductors L_1 and L_2, conduction and switching losses in switches S_1 and S_2, conduction and reverse recovery losses in diodes, and conduction losses in the ESR of the capacitors. The conduction losses in the inductors are calculated as

$$P_{L\_Cond} = \left(I_{L1,rms}{}^2 \times R_{L1,DCR}\right) + \left(I_{L2,rms}{}^2 \times R_{L2,DCR}\right) \tag{17}$$

The conduction and switching losses in the switches are calculated as

$$P_{S\_Cond} = \left(I_{S1,rms}{}^2 \times R_{DS,S1}\right) + \left(I_{S2,rms}{}^2 \times R_{DS,S2}\right) \tag{18}$$

$$P_{S\_Switching} = \left[\frac{1}{2} \times I_{L1,avg} \times V_{S1} \times \left(T_{on,S1} + T_{off,S1}\right) \times f_{sw}\right] + \left[\frac{1}{2} \times I_{L2,avg} \times V_{S2} \times \left(T_{on,S2} + T_{off,S2}\right) \times f_{sw}\right] \tag{19}$$

With similar diode used for D_1, D_2, D_3, and D_{out}, the

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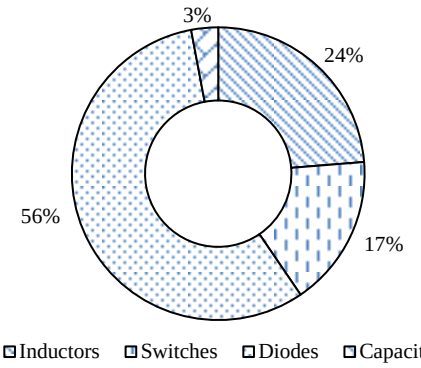

Fig. 12. Percentage distribution of losses in system components

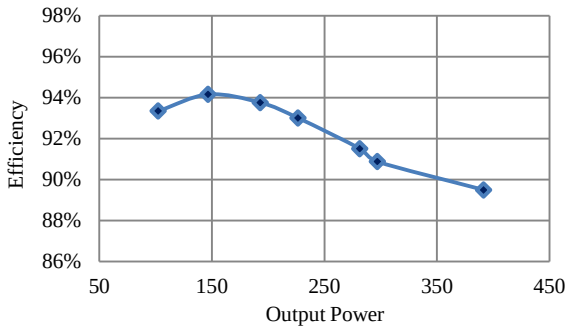

Fig. 13. Efficiency curve of the proposed converter

conduction and reverse recovery losses in the diodes can be calculated as

$$P_{D\_Cond} = 4 \times \left[\left(I_{D,avg} \times V_{F,D} \right) + \left({I_{D,rms}}^2 \times R_D \right) \right] \quad (20)$$

$$P_{D\_RR} = 4 \times \left[\frac{1}{2} \times \left(T_{RR} \times I_{RR} \right) \times V_D \times f_{sw} \right] \quad (21)$$

The conduction losses in the ESR of the capacitors can be calculated as

$$P_{C\_Cond} = \left[{I_{C1,rms}}^2 \times \left(R_{ESR1} + R_{ESR2} + R_{ESR3} + R_{ESR4} \right) \right] + \left[{I_{Cout,rms}}^2 \times R_{ESRout} \right] \quad (22)$$

The total loss in the proposed converter is given as

$$P_{Loss} = P_{L\_Cond} + P_{S\_Cond} + P_{S\_Switching} + P_{D\_Cond} + P_{D\_RR} + P_{C\_Cond} \quad (23)$$

The percentage distribution of losses in the system components is shown in Fig. 12. It is observed that the major percent of losses occur in the diodes which are about 56%. As there are 4 diodes in the converter, each diode has a loss of about 14%. As the diode losses increase, its junction temperature rises and decreases the forward voltage drop across it. This decrease in forward voltage drop reduces the power loss and helps in preventing a further increase in junction temperature which can lead to diode failure. In the worst case scenario, the losses in the selected diode were estimated to be within its power dissipation limits. The authors however would suggest using a plug in style heat sink like the 5768 series of aavid thermalloy to prevent the diode from any overheating and operate it at a temperature that is well below its maximum operating junction temperature. This particular heat sink contributes to a minimal increase in the volume of the converter.

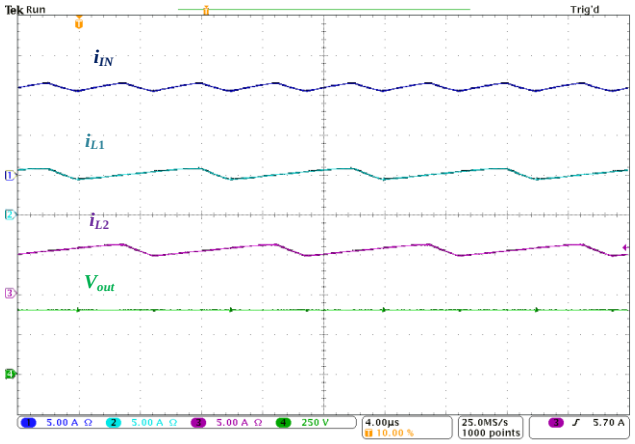

Fig. 14. Input current (i_{IN}), Inductor currents (i_{L1}, i_{L2}), and Output Voltage (V_{out})

Around 24% and 17% of the losses occur among the inductors and switches, respectively. The conduction losses in the inductors can be reduced by selecting an inductor with lower value of DCR (DC Resistance). The selected switches have similar conduction and switching losses. The losses in the capacitors are very small as the ESR of the film capacitors used is in the order of few milliohms and the rms currents are around 1A. Using (17)-(23), the theoretical efficiency of the proposed converter at 200W was around 96.8%. A 400W prototype was built and tested to validate the analytical results. An efficiency of 93.76% was observed at 200W of output power. The difference in the calculated and experimental efficiency can be accounted for the core losses in the inductors that were not considered in the calculated efficiency and the approximate approach to calculating component losses. The efficiency of the prototype over a wide range of output power is shown in Fig. 13. A maximum efficiency of 94.16% was achieved at a power rating of 150W.

The experimental waveforms are shown in Figs. 14-17. The experimental waveforms conform to simulation waveforms. Fig. 14 shows the input current, inductor currents i_{L1} and i_{L2}, and the output voltage of the converter. It can be observed that the input current is continuous and has a smaller ripple compared to that in inductor currents. The inductor currents are equal and are 180 degrees out of phase from each other as the two phases of the interleaved boost are operated in such way. The output voltage is 400V and the voltage ripple is almost negligible. Fig. 15 shows the inductor currents along with the gate signals of the switches. The voltages of switches S_1 and S_2 are shown in Fig. 16. The turn off voltage of both switches is around 100V as can be calculated from (13). The inductor current waveforms are decreasing during the turn off of their respective switches. The 180 degree out of phase operation of switches S_1 and S_2 can be clearly seen in the switch voltages.

The reverse blocking voltages of diode D_2 and output diode D_{out} are shown in Fig. 17. The maximum blocking voltage of the diodes is observed to be 200V which is same as that calculated using (15). Also the wave shape of both

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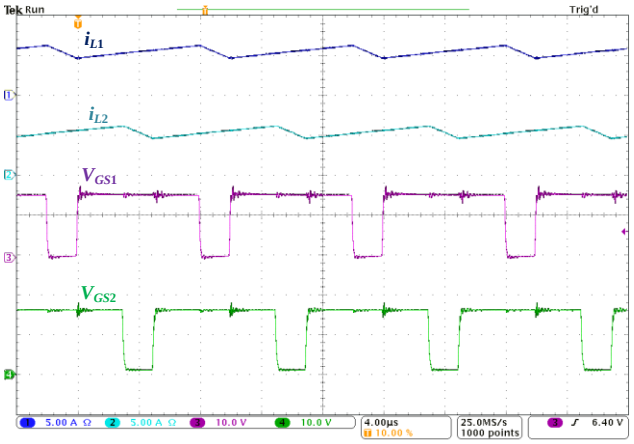

Fig. 15. Inductor currents (i_{L1}, i_{L2}) and Gate voltages (V_{GS1}, V_{GS2})

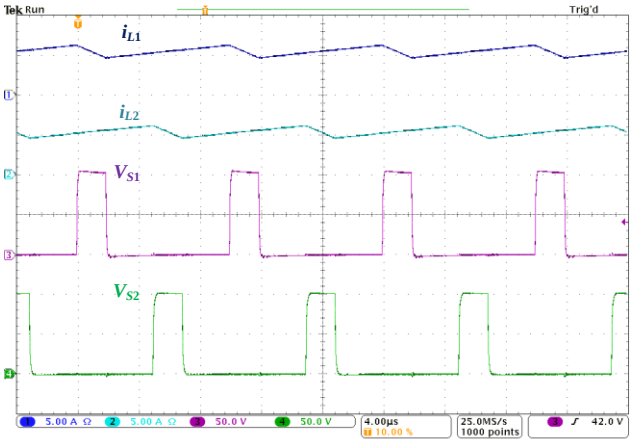

Fig. 16. Inductor currents (i_{L1}, i_{L2}) and Switch voltages (V_{S1}, V_{S2})

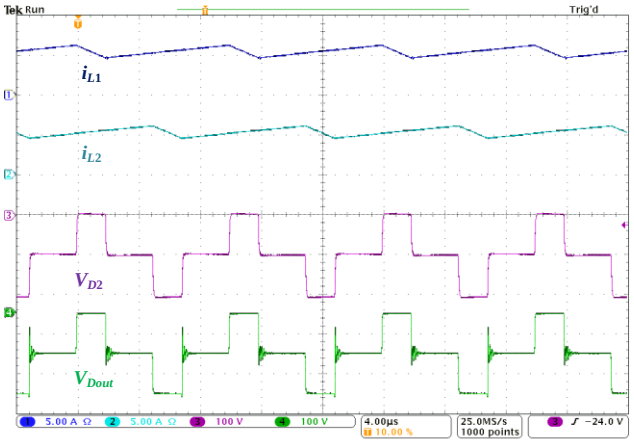

Fig. 17. Inductor currents (i_{L1}, i_{L2}) and Diode voltages (V_{D2}, V_{Dout})

diodes D_2 and D_{out} voltages are similar because they both are ON during mode I when the switch S_1 is turned OFF. Likewise, the wave shape of voltages of diodes D_1 and D_3 will be similar and have the maximum blocking voltage of 200V for the above test specifications. The experimental waveforms provided validate the converter operation and analysis. The proposed converter is capable of providing voltage gains high enough to step up the output voltage of renewable sources to the distribution level 400V DC.

TABLE IV
COMPARISON OF THE PROPOSED CONVERTER TO OTHER HIGH-VOLTAGE-GAIN CONVERTERS

Topology		**[8]**	**[9]**	**[10]**	**[11]**	**Proposed Converter**
V_{out}/V_{in}	C_{out}	$\frac{3-d}{1-d}$	$\frac{2}{1-d}$	$\frac{3+d}{1-d}$	$\frac{1}{d(1-d)}$	$\frac{4}{1-d}$
V_{switch}/V_{out}	S_1	$\frac{1}{3-d}$	$\frac{1}{2}$	$\frac{1}{3+d}$	$1-d$	$\frac{1}{4}$
	S_2	-	-	$\frac{1}{3+d}$	d	$\frac{1}{4}$
V_{diode}/V_{out}	D_1	$\frac{1}{3-d}$	$\frac{1}{2}$	$\frac{2}{3+d}$	$1-d$	$\frac{1}{2}$
	D_2	$\frac{1}{3-d}$	$\frac{1}{2}$	$\frac{2}{3+d}$	d	$\frac{1}{2}$
	D_3	$\frac{1}{3-d}$	-	-	d	$\frac{1}{2}$
	D_4	$\frac{1}{3-d}$	-	-	-	-
	D_o	-	$\frac{1}{2}$	$\frac{2}{3+d}$	-	$\frac{1}{2}$
V_{cap}/V_{out}	C_1	$\frac{1-d}{3-d}$	$\frac{1}{2}$	$\frac{1+d}{3+d}$	$1-d$	$\frac{3}{8}$
	C_2	$\frac{1}{3-d}$	$\frac{1}{2}$	$\frac{2}{3+d}$	d	$\frac{1}{8}$
	C_3	$\frac{1}{3-d}$	-	$\frac{2}{3+d}$	d	$\frac{1}{8}$
	C_4	$\frac{1}{3-d}$	-	-	-	$\frac{3}{8}$

VII. PROPOSED CONVERTER VS. HIGH-VOLTAGE-GAIN CONVERTERS USING BOOST STAGE AND VOLTAGE MULTIPLIER CIRCUITS

In this section, the proposed converter is compared to other high-voltage-gain converters using boost stage and voltage multiplier circuits. A comparison is made between the proposed converter and converters from [8-11] that have been discussed earlier in this paper. The comparison is based on the voltage gain of the converters along with the voltage stress on their components. To have a fair comparison, the voltage stress on its components has been normalized with respect to their output voltages. The comparison is summarized in Table IV. The proposed converter offers higher voltage gain, has lower voltage stress on its switches and diodes in comparison to all other converters. The major advantage with the proposed converter is the significantly smaller voltage ratings for its capacitors in comparison to other converters. This greatly contributes to cost and size reduction of the proposed converter.

The proposed converter is also compared to a high-voltage-gain converter using Dickson charge pump voltage multiplier cells that is very similar in structure and operation. The comparison of these two converters is shown in Table V. The high-voltage-gain converter using the Dickson charge pump voltage multiplier cells [19] will be referred to as reference converter in the following sections of the paper (see Fig. 1). Both converters mainly differ in terms of their component stresses. The converters are being compared in terms of component stress and size while both offer a voltage gain of

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TABLE V
COMPARISON OF THE PROPOSED CONVERTER TO THE REFERENCE CONVERTER

Component	Parameter	Reference Converter [19]	Proposed Converter
Input	Current	Continuous	Continuous
Inductor	Current	I_{L1}=6 A, I_{L2}=4 A	I_{L1}=5 A, I_{L2}=5 A
Switches	Voltage	V_{S1}=80 V, V_{S2}=80 V	V_{S1}=100 V, V_{S2}=100 V
	Duty Cycle	D_1=D_2=75%	D_1=D_2=80%
	Current	I_{S1}=6 A, I_{S2}=4 A	I_{S1}=5 A, I_{S2}=5 A
VM Capacitors	Capacitance for 1% voltage ripple	C_1=12.5 µF, C_2=6.25 µF, C_3=4.17 µF, C_4=3.125 µF	C_1=C_4=6.66 µF, C_2=C_3=20 µF
	Voltage	V_{C1}=80 V, V_{C2}=160 V, V_{C3}=240 V, V_{C4}=320 V	V_{C1}=V_{C4}=150 V, V_{C2}=V_{C3}=50 V
Diodes	Voltage	V_{D1}=160 V, V_{D2}=160 V, V_{D3}=160 V, V_{D4}=160 V, V_{Dout}=80 V	V_{D1}=200 V, V_{D2}=200 V, V_{D3}=200 V, V_{Dout}=200 V
Output Capacitor	Capacitance for 1V ripple	C_{out}=1.875 µF	C_{out}=1.875 µF
	Voltage	V_{Cout}=400 V	V_{Cout}=400 V

20, i.e., a 20V input is stepped up to 400V on the output side. Here in this comparison, both converters are sourced from a single source despite the fact that they could be powered from two independent sources.

Both converters achieve a high voltage gain by charging and discharging of the voltage multiplier capacitors. They offer continuous input current which can be owed to the two-phase interleaved boost topology on the input side. The proposed converter is symmetric, i.e., both the interleaved boost phases on the input side experience same voltage and current stresses. Also, some of the capacitors in the voltage multiplier circuit have similar voltage stress. This simplifies the effort and time during component selection of the system design. The switches in the proposed converter have a higher duty ratio as the proposed converter offers slightly lower gain. This leads to a slightly higher voltage stress across the switches compared to the reference topology.

The major difference in the converters being compared is in their voltage multiplier circuits. Apart from the output capacitor, both the reference converter and proposed converter have four voltage multiplier capacitors. The capacitors in the reference converter have linearly increasing voltage stress as observed from C_1 to C_4. The voltages of the capacitors C_1, C_2, C_3, and C_4 are 80V, 160V, 240V, and 320V respectively. For a 1% ripple voltage in the voltage multiplier capacitors, the required capacitance for C_1, C_2, C_3, and C_4 are 12.5 µF, 6.25 µF, 4.17 µF, and 3.125 µF, respectively. The proposed converter has smaller voltage rating for the voltage multiplier capacitors. Capacitors C_1, C_4 have a voltage stress of 150V and C_2, C_3 have a voltage stress of 50V. For a 1% ripple voltage in the voltage multiplier capacitors, the required capacitance for C_1, C_2, C_3, and C_4 are 6.66 µF, 20 µF, 20 µF, and 6.66 µF, respectively.

The proposed converter has a smaller size compared to the reference topology due to its voltage multiplier circuit capacitors. Ideally, this can be demonstrated by looking at the total energy of the voltage multiplier capacitors which can be calculated as follows.

$$E_{total} = \sum_{n=1}^{4} \frac{1}{2} \times C_n \times V_n^2 \qquad (24)$$

The total energy of the voltage multiplier capacitors of the reference converter is 0.4J while that of the proposed converter is 0.2J. It can be seen that the capacitors of the proposed converter hold only 50% of the energy compared to the reference converter. A more practical way to compare the converter size is by looking at the volume of selected voltage multiplier capacitors available in the market. The voltage multiplier capacitors were selected from "KEMET R60-Series Film Capacitors" such that they had the closest capacitance and voltage ratings to what was required. It was observed that the proposed converter had 44% smaller volume of voltage multiplier capacitors compared to the reference converter. Therefore the size of the proposed converter is smaller compared to the reference converter.

The proposed converter has one less diode compared to the reference converter. All the diodes experience the same reverse blocking voltage of 200V which is slightly higher than that of the diodes in the reference converter. This is because of the slightly higher duty ratio of the proposed converter compared to the reference converter. As the output ratings are the same, the output capacitors of both the converters are the same.

VIII. CONCLUSION

In this paper, a high-voltage-gain dc-dc converter is introduced that can offer a voltage gain of 20, i.e., to step up a 20V input to 400V output. The proposed converter is based on a two-phase interleaved boost and the modified Dickson charge pump voltage multiplier circuit. It can draw power from a single source as well as from two independent sources while offering continuous input current in both cases. This makes the converter well suited for renewable applications like solar. The proposed converter is symmetric, i.e., the semiconductor components experience same voltage and current stresses which therefore reduces the effort and time spent in the component selection during the system design. The proposed converter has smaller voltage multiplier capacitors compared to a reference converter based on Dickson charge pump voltage multiplier cells; hence it is smaller in size. The converter finds its application in integration of individual solar panels onto the 400V distribution bus in datacenters, telecom centers, dc buildings and microgrids.

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