Analysis and Design of an Input-Series Two-Transistor Forward Converter for High-Input Voltage Multiple-Output Applications

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***Abstract*—In this paper, an input-series two-transistor forward converter is proposed and investigated, which is aiming at the high-input voltage multiple-output applications. In this converter, all of the switches are operating synchronously, and the input voltage sharing (IVS) of each series-module is achieved automatically by the coupling of primary windings of the common forward integrated transformer. The active IVS processes are analyzed based on the model of the forward integrated transformer. Through the influence analysis when the mismatches in various series-modules are considered, design principles of the key parameters in each series-module are discussed to suppress the input voltage difference. Finally, a 96W laboratory-made prototype composed of two forward series-modules is built, and the feasibility of the proposed method and the theoretical analysis are verified by the experimental results.**

***Index Terms*—Input-series, integrated-transformer, multiple-output, two-transistor forward.**

I. Introduction

PRSENTLY, the applications of high dc input voltage are gradually increasing. For example, in the 1500Vdc power supply of the metro vehicle, the maximum input voltage may be over 1800V, in the high-speed train electrical systems, the dc supply voltage is up to 2000-4000V, and in the coalmining industry, input voltage of the high voltage frequency converter will be 2000-3000V. For the converters with high voltage input, the large voltage stress of switches represents a major design challenge. To reduce the voltage stress, one solution is to connect the switches in series, but some special passive or active balancing methods must be introduced to achieve voltage balancing of the series switches, which cause the additional losses and restrict the switching frequency [1]. Another solution is the multilevel dc/dc converters, however, as the number of "level" increases, the number of the clamping diodes or flying capacitors increases, and the associated control becomes more complex [2], [3]. Generally, the multilevel converters aren't suitable for the medium or low power applications. A third option is the input-series converters, which can solve the high-voltage problems efficiently [4]-[6].

For the input-series converters, the most important issues are to ensure their input voltage sharing (IVS) [7], [8]. To achieve IVS, many special control strategies are proposed and introduced in the input-series converters, which have been the most widely investigated [8]-[16]. However, in these input-series converters, a dedicated IVS controller must be used, which results in the increasing complexity of the associated control and the decreasing reliability of the whole system. The multiple-output converters are usually designed for the medium or low power applications, therefore, the simplicity and high-reliability of the whole system are very important.

To simplify the circuit system, some input-series converters without any special IVS controller have been investigated. In these converters, the basic common-duty-ratio control strategy is adopted, and IVS can be achieved automatically. For example, a forward converter is implemented in [17], the flyback converters are investigated in [18] and [19], and the full-bridge converters are presented in [2], [20] and [21]. However, due to the connection structure in their output circuits, these converters are not suitable for the multiple-output applications.

The input-series converters with a common integrated transformer have also been presented, which can be used in the multiple-output applications. The typical investigations are as follows.

In [22]-[24], the converters with two forward series-modules operating interleaved are investigated. In these converters, IVS can be achieved due to the volt-second balance between the two

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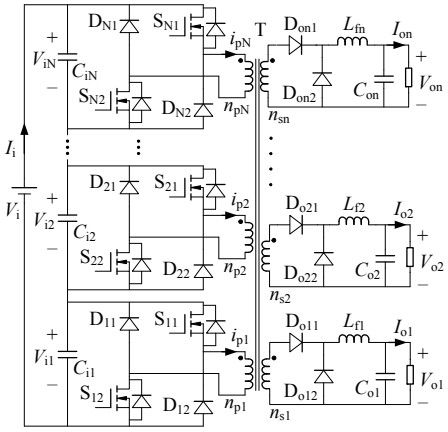

Fig.1. The input-series multiple-output two-transistor forward converter.

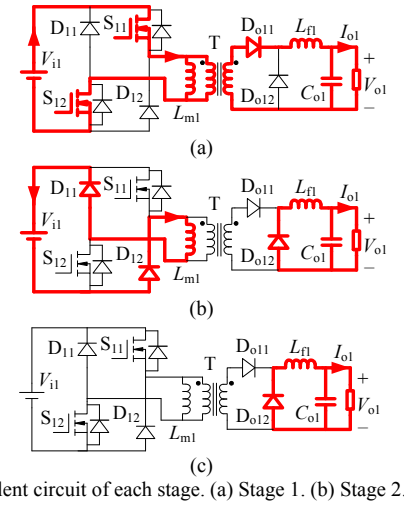

Fig. 2. Equivalent circuit of each stage. (a) Stage 1. (b) Stage 2. (c) Stage 3.

primary windings of the integrated transformer. However, number of their series-modules cannot be increased arbitrarily because of the interleaved operating of each series-module.

In [25] and [26], the converters with two full-bridge series-modules are investigated. In these converters, IVS can be achieved automatically when the series-modules operate synchronously. This structure is suitable for the multiple-output applications when flyback or forward topology is adopted in each series-module. However, these full-bridge converters are used in high power applications, so the input filter capacitance is much larger, and the input voltage differences caused by the asynchronous operating of each series-module can be ignored, which cannot be ignored in the flyback or forward converters.

Based on the structure in [25] and [26], an input-series flyback converter is investigated in [27]. In this converter, IVS can be achieved automatically by the coupling of each primary winding of the flyback integrated transformer. However, the coupling of primary windings only occurs in the stage when the switches are turning on, so active IVS cannot be achieved when the switches are turning off. Moreover, the voltage difference of the switches may appear due to the tolerance features of the absorbing circuit in various series-modules.

In this paper, an input-series multiple-output two-transistor forward converter is proposed and investigated based on the structure in [25]-[27]. The proposed converter is suitable for the high-input voltage multiple-output applications, which is the same as the converter in [27]. However, the active IVS of the proposed converter is achieved by the coupling of each primary winding of the forward integrated transformer, which occurs both in the stages when the switches are turning on and off. Therefore, compared to the converter in [27], the active IVS can be achieved both in the stages when the switches are turning on and off. Furthermore, in the proposed converter, the voltage of each switch is equal to the input voltage of each series-module, so voltage balancing of the switches can also be achieved, which is another advantage compared to the converter in [27]. The rest of this paper is organized as follows. In section II, the proposed converter is introduced, and its active IVS processes when the switches are turning on and off are analyzed respectively. In section III, the input voltage differences are analyzed when the tolerance features of the key parameters are considered and when the series-modules are operating asynchronously, from which design principles of the key parameters are discussed. The proposed method and theoretical analysis are verified by the experimental results in section IV. Finally, conclusions are given in section V.

II. The Proposed Converter and Its IVS Processes

A. The Proposed Converter

The proposed input-series multiple-output two-transistor forward converter is shown in Fig.1, where the series-modules (the number is N, N≥1) employ an integrated transformer T and a common set of output circuits (the number is n, n≥1). V_i and I_i are the input voltage and current, V_{i1}, V_{i2}, ..., V_{iN} are the input voltage of the series-modules, C_{i1}, C_{i2}, ..., C_{iN} (C_{i1}=C_{i2}=...=C_{iN}=C_i) are the input filter capacitors, L_{f1}, L_{f2}, ..., L_{fn} and C_{o1}, C_{o2}, ..., C_{on} are the output filter inductors and capacitors, and V_{o1}, V_{o2}, . . ., V_{on} are the output voltage. In the integrated transformer, n_{p1}, n_{p2}, ..., n_{pN} (n_{p1}=n_{p2}=...=n_{pN}) are the turns of primary windings, and n_{s1}, n_{s2}, ..., n_{sn} are the turns of secondary windings. In this converter, all of the switches are turned on and off synchronously, and without any additional control strategy, the active IVS of each series-module can be achieved by the coupling of each primary winding of the integrated transformer.

To facilitate the IVS analysis, the operational process of this converter in ideal conditions is analyzed as follows. In ideal conditions, the voltage and current in each series-module are identical, so to simplify the analysis, N=1 and n=1 are considered here. It can be seen that the proposed converter is equivalent to a traditional two-transistor forward dc/dc converter when N=1. During one switching period, there are three main operational stages, and the equivalent circuit of each stage is shown in Fig.2, where L_{m1} is the equivalent excitation inductance of the transformer T.

Stage 1 (t_0~t_1): At t_0, S_{11} and S_{12} are turned on. The input energy is transferred to the load through the transformer. In the output circuit, D_{o11} is turning on, and D_{o12} is turning off.

Stage 2 (t_1~t_2): At t_1, S_{11} and S_{12} are turned off. The energy of L_{m1} is transferred back to the input side, and the transformer

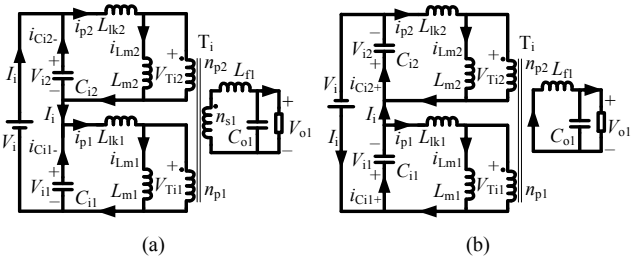

Fig.3. Simplified equivalent circuits. (a) Stage 1. (b) Stage 2.

achieves magnetic reset in this stage. In the output circuit, D_{o11} is turning off, D_{o12} is turning on, and the output energy is provided by the output filter inductors and capacitors.

Stage 3 (t_2~t_3): At t_2, the current of L_{m1} reduces to zero, and the transformer has achieved magnetic reset.

At t_3, S_{11} and S_{12} are turned on again, and the converter begins to operate in the next switching period.

For the proposed converter, the coupling of the primary windings will appear in stage 1 and 2 during one switching period. Therefore, the active IVS processes in these two stages are analyzed respectively in this section.

To simplify the analysis, it is assumed that: 1) the number of series-modules "N=2" is considered, 2) coupling of each winding in primary side of the integrated transformer is independent of the output circuits, so the number of output circuits "n=1" is considered, 3) the output is considered as a constant voltage source due to the large output filter capacitance, 4) the conduction resistance of each switch is ignored, and 5) the difference of each parameter in the series-modules is ignored. The IVS processes are analyzed based on the simplified equivalent circuits in Fig.3, in which the model of the forward integrated transformer T is included, where L_{lk1}, L_{lk2} (L_{lk1}=L_{lk2}=L_{lk}) are the equivalent leakage inductance, L_{m1}, L_{m2} (L_{m1}=L_{m2}=L_m) are the equivalent excitation inductance, and T_i is the ideal transformer (for the ideal transformer, because of n_{p1}=n_{p2}, it is considered that: V_{Ti1}=V_{Ti2}=V_{Ti}).

B. The Active IVS Process in Stage 1

In stage 1, the time t_m is defined, and it is assumed that: before t_m, I_i=i_{p1}=i_{p2} (i_{p1}, i_{p2} are the current in primary sides of T), V_{i1}=V_{i2}=V_i/2, and at t_m, $I_i(t_m)$=$i_{p1}(t_m)$=$i_{p2}(t_m)$, $V_{i1}(t_m)$=V_i/2+ΔV_i, $V_{i2}(t_m)$=V_i/2-ΔV_i, where ΔV_i>0. So after t_m, the following relationships can be obtained from Fig.3 (a):

$$\begin{cases} i_{p1}(t-t_m)=i_{p1}(t_m)+\int_{t_m}^{t}\dfrac{V_{i1}(t-t_m)-V_{Ti}}{L_{lk}}dt \\ i_{p2}(t-t_m)=i_{p2}(t_m)+\int_{t_m}^{t}\dfrac{V_{i2}(t-t_m)-V_{Ti}}{L_{lk}}dt \end{cases} \tag{1}$$

$$i_{p1}(t-t_m)+i_{p2}(t-t_m)=2i_{p1}(t_m)+\int_{t_m}^{t}\left(\frac{V_i}{L_{lk}+L_m}+\frac{V_{Ti}-nV_{o1}}{n^2L_{f1}}\right)dt \tag{2}$$

$$I_i(t-t_m)=I_i(t_m)+\int_{t_m}^{t}\left[\frac{V_i}{2(L_{lk}+L_m)}+\frac{V_{Ti}-nV_{o1}}{2n^2L_{f1}}\right]dt \tag{3}$$

where n=n_{p1}/n_{S1}.

For the discharging current of C_{i1} and C_{i2} (i_{Ci1-}=i_{p1}-I_i, i_{Ci2-}=i_{p2}-I_i), it can be obtained from (1) that:

$$\Delta I_{Ci12-}=i_{Ci1-}(t-t_m)-i_{Ci2-}(t-t_m)=\int_{t_m}^{t}\frac{2\Delta V_i(t-t_m)}{L_{lk}}dt \tag{4}$$

From (4), it can be seen after t_m that: 1) when V_{i1}>V_{i2} (ΔV_i>0), i_{Ci1-}>i_{Ci2-} will appear, which can help accelerate the discharging of C_{i1}, and decelerate the discharging of C_{i2}, and 2) as L_{lk} decreases, ΔI_{Ci12-} will increase and the voltage balance between C_{i1} and C_{i2} will be achieved more easily.

For C_{i1}, it can be obtained after t_m that:

$$C_i\frac{d\Delta V_i(t-t_m)}{dt}=-i_{Ci1-}(t-t_m)=I_i(t-t_m)-i_{p1}(t-t_m) \tag{5}$$

From (2) and (4), i_{p1} can be calculated as follows:

$$i_{p1}(t-t_m)=i_{p1}(t_m)+\int_{t_m}^{t}\left[\frac{V_i}{2(L_{lk}+L_m)}+\frac{V_{Ti}-nV_{o1}}{2n^2L_{f1}}+\frac{\Delta V_i(t-t_m)}{L_{lk}}\right]dt \tag{6}$$

From (3), (5) and (6), the following equation is obtained:

$$\frac{d^2\Delta V_i(t-t_m)}{dt^2}+\frac{\Delta V_i(t-t_m)}{L_{lk}C_i}=0 \tag{7}$$

At t_m, $\Delta V_i(t_m)$=ΔV_i, $i_{Ci1-}(t_m)$=0. So the solution of (7) is:

$$\Delta V_i(t-t_m)=\Delta V_i\cos\frac{t-t_m}{\sqrt{L_{lk}C_i}} \tag{8}$$

From (8), the expressions of V_{i1} and V_{i2} after t_m are:

$$\begin{cases} V_{i1}(t-t_m)=\dfrac{V_i}{2}+\Delta V_i(t-t_m)=\dfrac{V_i}{2}+\Delta V_i\cos\dfrac{t-t_m}{\sqrt{L_{lk}C_i}} \\ V_{i2}(t-t_m)=\dfrac{V_i}{2}-\Delta V_i(t-t_m)=\dfrac{V_i}{2}-\Delta V_i\cos\dfrac{t-t_m}{\sqrt{L_{lk}C_i}} \end{cases} \tag{9}$$

C. The Active IVS Process in Stage 2

In stage 2, the time t_n is defined, and it is assumed that: before t_n, -I_i=i_{p1}=i_{p2}, V_{i1}=V_{i2}=V_i/2, and at t_n, -$I_i(t_n)$=$i_{p1}(t_n)$=$i_{p2}(t_n)$, $V_{i1}(t_n)$=V_i/2+ΔV_i, $V_{i2}(t_n)$=V_i/2-ΔV_i. After t_n, the following relationships can be obtained from Fig.3 (b):

$$\begin{cases} i_{p1}(t-t_n)=i_{p1}(t_n)-\int_{t_n}^{t}\dfrac{V_{i1}(t-t_n)+V_{Ti}}{L_{lk}}dt \\ i_{p2}(t-t_n)=i_{p2}(t_n)-\int_{t_n}^{t}\dfrac{V_{i2}(t-t_n)+V_{Ti}}{L_{lk}}dt \end{cases} \tag{10}$$

$$i_{p1}(t-t_n)+i_{p2}(t-t_n)=2i_{p1}(t_n)-\int_{t_n}^{t}\frac{V_i}{L_{lk}+L_m}dt \tag{11}$$

$$I_i(t-t_n)=I_i(t_n)+\int_{t_n}^{t}\frac{V_i}{2(L_{lk}+L_m)}dt \tag{12}$$

For the charging current of C_{i1} and C_{i2} (i_{Ci1+}=i_{p1}+I_i, i_{Ci2+}=i_{p2}+I_i), it can be obtained from (10) that:

$$\Delta I_{Ci12+}=i_{Ci1+}(t-t_n)-i_{Ci2+}(t-t_n)=-\int_{t_n}^{t}\frac{2\Delta V_i(t-t_n)}{L_{lk}}dt \tag{13}$$

From (13), it can be seen after t_n that: 1) when V_{i1}>V_{i2} (ΔV_i>0), i_{Ci1+}<i_{Ci2+} will appear, which can help decelerate the charging of C_{i1} and accelerate the charging of C_{i2}, and 3) as L_{lk} decreases, -ΔI_{Ci12+} will increase and the voltage balance between C_{i1} and C_{i2} will be achieved more easily.

For C_{i1}, it can be obtained after t_n that:

$$C_i\frac{d\Delta V_i(t-t_n)}{dt}=i_{Ci1+}(t-t_n)=I_i(t-t_n)+i_{p1}(t-t_n) \tag{14}$$

From (11) and (13), i_{p1} can be calculated as follows:

$$i_{p1}(t-t_n)=i_{p1}(t_n)-\int_{t_n}^{t}\left[\frac{V_i}{2(L_{lk}+L_m)}+\frac{\Delta V_i(t-t_n)}{L_{lk}}\right]dt \tag{15}$$

From (12), (14) and (15), a similar differential equation can

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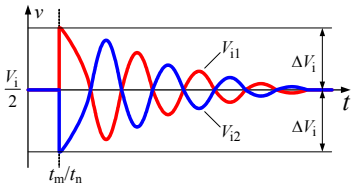

Fig.4. Active IVS processes.

be obtained:

$$\frac{\mathrm{d}^2\Delta V_{\mathrm{i}}(t-t_{\mathrm{n}})}{\mathrm{d}t^2}+\frac{\Delta V_{\mathrm{i}}(t-t_{\mathrm{n}})}{L_{\mathrm{lk}}C_{\mathrm{i}}}=0 \tag{16}$$

At t_n, $\Delta V_i(t_n)=\Delta V_i$, $i_{Ci1+}(t_n)=0$. Similarly, the expressions of V_{i1} and V_{i2} after t_n can be obtained from (16):

$$\begin{cases} V_{\mathrm{i1}}(t-t_{\mathrm{n}})=\dfrac{V_{\mathrm{i}}}{2}+\Delta V_{\mathrm{i}}(t-t_{\mathrm{n}})=\dfrac{V_{\mathrm{i}}}{2}+\Delta V_{\mathrm{i}}\cos\dfrac{t-t_{\mathrm{n}}}{\sqrt{L_{\mathrm{lk}}C_{\mathrm{i}}}} \\ V_{\mathrm{i2}}(t-t_{\mathrm{n}})=\dfrac{V_{\mathrm{i}}}{2}-\Delta V_{\mathrm{i}}(t-t_{\mathrm{n}})=\dfrac{V_{\mathrm{i}}}{2}-\Delta V_{\mathrm{i}}\cos\dfrac{t-t_{\mathrm{n}}}{\sqrt{L_{\mathrm{lk}}C_{\mathrm{i}}}} \end{cases} \tag{17}$$

As shown in Fig.4, the active IVS processes of this converter can be obtained from (9) and (17). It can be seen that if there is a difference between V_{i1} and V_{i2}, a high frequency resonance will appear. Because of the resistance of each series-module, the amplitude decreases in each resonant period. The resonant period is given in (18), it can be seen that the IVS will be achieved more speedily as L_{lk} decreases.

$$T_{\mathrm{r}}=2\pi\sqrt{L_{\mathrm{lk}}C_{\mathrm{i}}} \tag{18}$$

From the above analysis, it can be seen that: without any additional control strategy, active IVS of this converter can be achieved by the coupling of windings in primary sides of the forward integrated transformer. Furthermore, the voltage stress of each switch is equal to the input voltage of each two-transistor forward series-module, so voltage balancing of the switches can also be achieved in this converter.

III. Analysis and Suppression of the Input Voltage Difference

In section II, the IVS processes are discussed in ideal conditions. Generally, the input voltage difference (ΔV_i) cannot appear because it is assumed that the series-modules have the same parameters. However, in the real conditions, the parameters in various series-modules cannot be identical absolutely, so the input voltage difference will appear.

Active IVS of this converter can be realized when the input voltage difference appears. However, due to the input voltage difference, current difference in primary sides of the integrated transformer will also appear in the IVS process. If the current difference is large enough, efficiency of the converter will decrease obviously because the serious-module with lower input voltage becomes a load for the other one. It can be easily obtained that: due to the resistance of each series-module, the current difference will increase as the input voltage difference increases. Therefore, the input voltage difference should be avoided or reduced.

A. Analysis when Differences of the Key Parameters Appear in Various Series-Modules

The following analysis is based on the differences appearing between C_{i1} and C_{i2}, L_{lk1} and L_{lk2}, L_{m1} and L_{m2}.

Firstly, it is assumed that there is no input voltage difference before t_0. From Fig.3 (a), it can be obtained after t_0:

$$\begin{cases} C_{\mathrm{i1}}\dfrac{\mathrm{d}V_{\mathrm{i1}}(t-t_0)}{\mathrm{d}t}=I_{\mathrm{i}}(t-t_0)-i_{\mathrm{p1}}(t-t_0) \\ C_{\mathrm{i2}}\dfrac{\mathrm{d}V_{\mathrm{i2}}(t-t_0)}{\mathrm{d}t}=I_{\mathrm{i}}(t-t_0)-i_{\mathrm{p2}}(t-t_0) \end{cases} \tag{19}$$

$$\begin{cases} i_{\mathrm{p1}}(t-t_0)=\dfrac{i_{\mathrm{Lf1}}(t_0)}{2n}+\int_{t_0}^{t}[\dfrac{V_{\mathrm{i1}}(t-t_0)}{L_{\mathrm{lk1}}+L_{\mathrm{m1}}}+\dfrac{V_{\mathrm{Ti}}-nV_{\mathrm{o1}}}{2n^2L_{\mathrm{f1}}}]\mathrm{d}t \\ i_{\mathrm{p2}}(t-t_0)=\dfrac{i_{\mathrm{Lf1}}(t_0)}{2n}+\int_{t_0}^{t}[\dfrac{V_{\mathrm{i2}}(t-t_0)}{L_{\mathrm{lk2}}+L_{\mathrm{m2}}}+\dfrac{V_{\mathrm{Ti}}-nV_{\mathrm{o1}}}{2n^2L_{\mathrm{f1}}}]\mathrm{d}t \end{cases} \tag{20}$$

$$I_{\mathrm{i}}(t-t_0)=\frac{i_{\mathrm{Lf1}}(t_0)}{2n}+\int_{t_0}^{t}[\frac{V_{\mathrm{i}}}{L_{\mathrm{m1}}+L_{\mathrm{lk1}}+L_{\mathrm{m2}}+L_{\mathrm{lk2}}}+\frac{V_{\mathrm{Ti}}-nV_{\mathrm{o1}}}{2n^2L_{\mathrm{f1}}}]\mathrm{d}t \tag{21}$$

From (19), (20) and (21), the following equations can be obtained:

$$\begin{cases} \dfrac{\mathrm{d}^2V_{\mathrm{i1}}(t-t_0)}{\mathrm{d}t^2}+\dfrac{V_{\mathrm{i1}}(t-t_0)}{(L_{\mathrm{lk1}}+L_{\mathrm{m1}})C_{\mathrm{i1}}}=\dfrac{V_{\mathrm{i}}}{(L_{\mathrm{lk1}}+L_{\mathrm{m1}}+L_{\mathrm{lk2}}+L_{\mathrm{m2}})C_{\mathrm{i1}}} \\ \dfrac{\mathrm{d}^2V_{\mathrm{i2}}(t-t_0)}{\mathrm{d}t^2}+\dfrac{V_{\mathrm{i2}}(t-t_0)}{(L_{\mathrm{lk2}}+L_{\mathrm{m2}})C_{\mathrm{i2}}}=\dfrac{V_{\mathrm{i}}}{(L_{\mathrm{lk1}}+L_{\mathrm{m1}}+L_{\mathrm{lk2}}+L_{\mathrm{m2}})C_{\mathrm{i2}}} \end{cases} \tag{22}$$

At t_0, $V_{i1}(t_0)=V_{i2}(t_0)=V_i/2$, $i_{Ci1-}(t_0)=i_{Ci2-}(t_0)=0$, so it can be calculated from (22) that:

$$\begin{cases} V_{\mathrm{i1}}(t-t_0)=\dfrac{V_{\mathrm{i}}}{2}+\dfrac{V_{\mathrm{i}}}{2}\dfrac{L_{\mathrm{lk1}}+L_{\mathrm{m1}}-L_{\mathrm{lk2}}-L_{\mathrm{m2}}}{L_{\mathrm{lk1}}+L_{\mathrm{m1}}+L_{\mathrm{lk2}}+L_{\mathrm{m2}}}(1-\cos\dfrac{t-t_0}{\sqrt{(L_{\mathrm{lk1}}+L_{\mathrm{m1}})C_{\mathrm{i1}}}}) \\ V_{\mathrm{i2}}(t-t_0)=\dfrac{V_{\mathrm{i}}}{2}-\dfrac{V_{\mathrm{i}}}{2}\dfrac{L_{\mathrm{lk1}}+L_{\mathrm{m1}}-L_{\mathrm{lk2}}-L_{\mathrm{m2}}}{L_{\mathrm{lk1}}+L_{\mathrm{m1}}+L_{\mathrm{lk2}}+L_{\mathrm{m2}}}(1-\cos\dfrac{t-t_0}{\sqrt{(L_{\mathrm{lk2}}+L_{\mathrm{m2}})C_{\mathrm{i2}}}}) \end{cases} \tag{23}$$

Secondly, it is assumed that there is no input voltage difference before t_1. From Fig.3 (b), it can be obtained after t_1:

$$\begin{cases} C_{\mathrm{i1}}\dfrac{\mathrm{d}V_{\mathrm{i1}}(t-t_1)}{\mathrm{d}t}=I_{\mathrm{i}}(t-t_1)+i_{\mathrm{p1}}(t-t_1) \\ C_{\mathrm{i2}}\dfrac{\mathrm{d}V_{\mathrm{i2}}(t-t_1)}{\mathrm{d}t}=I_{\mathrm{i}}(t-t_1)+i_{\mathrm{p2}}(t-t_1) \end{cases} \tag{24}$$

$$\begin{cases} i_{\mathrm{p1}}(t-t_1)=i_{\mathrm{Lm1}}(t_1)-\int_{t_1}^{t}\dfrac{V_{\mathrm{i1}}(t-t_1)}{L_{\mathrm{lk1}}+L_{\mathrm{m1}}}\mathrm{d}t \\ i_{\mathrm{p2}}(t-t_1)=i_{\mathrm{Lm2}}(t_1)-\int_{t_1}^{t}\dfrac{V_{\mathrm{i2}}(t-t_1)}{L_{\mathrm{lk2}}+L_{\mathrm{m2}}}\mathrm{d}t \end{cases} \tag{25}$$

$$-I_{\mathrm{i}}(t-t_1)=i_{\mathrm{Lm1}}(t_1)-\int_{t_1}^{t}\frac{V_{\mathrm{i}}}{L_{\mathrm{m1}}+L_{\mathrm{lk1}}+L_{\mathrm{m2}}+L_{\mathrm{lk2}}}\mathrm{d}t \tag{26}$$

where $i_{Lm1}(t_1)=i_{Lm2}(t_1)$.

From (24), (25) and (26), the similar equations can be obtained:

$$\begin{cases} \dfrac{\mathrm{d}^2V_{\mathrm{i1}}(t-t_1)}{\mathrm{d}t^2}+\dfrac{V_{\mathrm{i1}}(t-t_1)}{(L_{\mathrm{lk1}}+L_{\mathrm{m1}})C_{\mathrm{i1}}}=\dfrac{V_{\mathrm{i}}}{(L_{\mathrm{lk1}}+L_{\mathrm{m1}}+L_{\mathrm{lk2}}+L_{\mathrm{m2}})C_{\mathrm{i1}}} \\ \dfrac{\mathrm{d}^2V_{\mathrm{i2}}(t-t_1)}{\mathrm{d}t^2}+\dfrac{V_{\mathrm{i2}}(t-t_1)}{(L_{\mathrm{lk2}}+L_{\mathrm{m2}})C_{\mathrm{i2}}}=\dfrac{V_{\mathrm{i}}}{(L_{\mathrm{lk1}}+L_{\mathrm{m1}}+L_{\mathrm{lk2}}+L_{\mathrm{m2}})C_{\mathrm{i2}}} \end{cases} \tag{27}$$

At t_1, $V_{i1}(t_1)=V_{i2}(t_1)=V_i/2$, $i_{Ci1+}(t_1)=i_{Ci2+}(t_1)=0$. So it can be calculated from (27) that:

$$\begin{cases} V_{\mathrm{i1}}(t-t_1)=\dfrac{V_{\mathrm{i}}}{2}+\dfrac{V_{\mathrm{i}}}{2}\dfrac{L_{\mathrm{lk1}}+L_{\mathrm{m1}}-L_{\mathrm{lk2}}-L_{\mathrm{m2}}}{L_{\mathrm{lk1}}+L_{\mathrm{m1}}+L_{\mathrm{lk2}}+L_{\mathrm{m2}}}(1-\cos\dfrac{t-t_1}{\sqrt{(L_{\mathrm{lk1}}+L_{\mathrm{m1}})C_{\mathrm{i1}}}}) \\ V_{\mathrm{i2}}(t-t_1)=\dfrac{V_{\mathrm{i}}}{2}-\dfrac{V_{\mathrm{i}}}{2}\dfrac{L_{\mathrm{lk1}}+L_{\mathrm{m1}}-L_{\mathrm{lk2}}-L_{\mathrm{m2}}}{L_{\mathrm{lk1}}+L_{\mathrm{m1}}+L_{\mathrm{lk2}}+L_{\mathrm{m2}}}(1-\cos\dfrac{t-t_1}{\sqrt{(L_{\mathrm{lk2}}+L_{\mathrm{m2}})C_{\mathrm{i2}}}}) \end{cases} \tag{28}$$

From (23) and (28), it can be seen that the input voltage difference will increase as the difference between L_{m1} and L_{m2} (or L_{lk1} and L_{lk2}) increases. If the coupling in primary sides of

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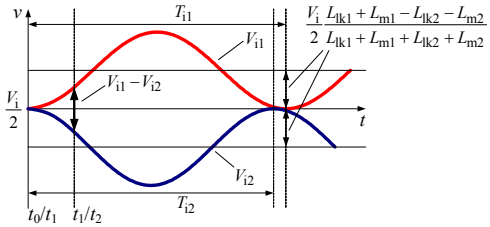

Fig.5. Vary curves of V_{i1} and V_{i2} when the differences of capacitances and inductances are considered.

the integrated transformer isn't considered here, from (23) and (28), the varying curves of V_{i1} and V_{i2} after t_0 (or t_1) can be obtained as shown in Fig.5, where T_{i1}, T_{i2} are their resonant periods as shown in (29), and T_{i1}, T_{i2} are much larger than the turning on (or off) time of the switches.

$$T_{i1}=2\pi\sqrt{(L_{m1}+L_{lk1})C_{i1}}\ ,\ T_{i2}=2\pi\sqrt{(L_{m2}+L_{lk2})C_{i2}} \tag{29}$$

B. Analysis when the Switches are Turned on and off Asynchronously in Various Series-Modules

Due to the tolerance features of the switches and their driving circuits, the switches cannot be turned on or off at the same time absolutely, which will also result in the input voltage difference. Therefore, the influence is analyzed as follows when the series-modules are operating asynchronously, where the maximum differences of turning on and off time between the switches in various series-modules are defined as ΔT_{on} and ΔT_{off}, and the difference between the two switches in the same series-module is ignored.

It is assumed that: before t_0, $V_{i1}=V_{i2}=V_i/2$, S_{21}, S_{22} are turned on at t_0, and S_{11}, S_{12} are turned on at $t_0+\Delta T_{on}$. So after t_0, V_{i1} begins to increase, and V_{i2} begins to decrease. From t_0 to $t_0+\Delta T_{on}$, it can be obtained from Fig.2 (a):

$$\begin{cases} C_i\dfrac{dV_{i1}(t-t_0)}{dt}=I_i(t-t_0)-i_{p1}(t-t_0) \\ C_i\dfrac{dV_{i2}(t-t_0)}{dt}=-C_i\dfrac{dV_{i1}(t-t_0)}{dt}=I_i(t-t_0)-i_{p2}(t-t_0) \\ i_{p1}(t-t_0)=0 \\ i_{p2}(t-t_0)=\dfrac{i_{Lf1}}{n}+\displaystyle\int_{t_0}^{t}\frac{V_{i2}(t-t_0)}{L_{lk}+L_m}dt \end{cases} \tag{30}$$

Generally, ΔT_{on} is much smaller than the duration from t_0 to t_1, so the current changing of L_{f1} can be ignored from t_0 to $t_0+\Delta T_{on}$. Therefore, it can be obtained from (30) that:

$$\frac{d^2V_{i1}(t-t_0)}{dt^2}+\frac{V_{i1}(t-t_0)}{2(L_{lk}+L_m)C_i}=\frac{V_i}{2(L_{lk}+L_m)C_i} \tag{31}$$

Equation (31) has the initial data that: $V_{i1}(t_0)=V_i/2$, $i_{p2}(t_0)=I_i(t_0)=i_{Lf1}(t_0)/n$. Therefore, its solution is:

$$\begin{aligned} V_{i1}(t-t_0)=&\frac{V_i}{2}+\frac{V_i}{2}\left(1-\cos\frac{t-t_0}{\sqrt{2(L_{lk}+L_m)C_i}}\right) \\ &+I_i(t_0)\sqrt{\frac{2(L_{lk}+L_m)}{C_i}}\sin\frac{t-t_0}{\sqrt{2(L_{lk}+L_m)C_i}} \end{aligned} \tag{32}$$

It is assumed that: before t_1, $V_{i1}=V_{i2}=V_i/2$, S_{11}, S_{12} are turned off at t_1, and S_{21}, S_{22} are turned off at $t_1+\Delta T_{off}$. So after t_1, V_{i1} begins to increase, and V_{i2} begins to decrease. From t_1 to $t_1+\Delta T_{off}$, it can be obtained from Fig.2 (a):

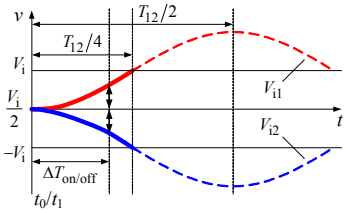

Fig.6. Vary curves of V_{i1} and V_{i2} when the switches in various series-modules are operating asynchronously.

$$\begin{cases} C_i\dfrac{dV_{i1}(t-t_1)}{dt}=I_i(t-t_1)-i_{p1}(t-t_1) \\ C_i\dfrac{dV_{i2}(t-t_1)}{dt}=-C_i\dfrac{dV_{i1}(t-t_1)}{dt}=I_i(t-t_1)-i_{p2}(t-t_1) \\ i_{p1}(t-t_1)=0 \\ i_{p2}(t-t_1)=\dfrac{i_{Lf1}}{n}+i_{Lm1}(t_1)+\displaystyle\int_{t_1}^{t}\frac{V_{i2}(t-t_1)}{L_{lk}+L_m}dt \end{cases} \tag{33}$$

The current changing of L_{f1} and L_{m1} is also ignored from t_1 to $t_1+\Delta T_{off}$ due to the small duration of ΔT_{off}, so it can be obtained from (33) that:

$$\frac{d^2V_{i1}(t-t_1)}{dt^2}+\frac{V_{i1}(t-t_1)}{2(L_{lk}+L_m)C_i}=\frac{V_i}{2(L_{lk}+L_m)C_i} \tag{34}$$

Equation (34) has the initial data that: $V_{i1}(t_1)=V_i/2$, $i_{p2}(t_1)=I_i(t_1)=i_{Lf1}(t_1)/n+i_{Lm1}(t_1)$. Therefore, its solution is:

$$\begin{aligned} V_{i1}(t-t_1)=&\frac{V_i}{2}+\frac{V_i}{2}\left(1-\cos\frac{t-t_1}{\sqrt{2(L_{lk}+L_m)C_i}}\right) \\ &+I_i(t_1)\sqrt{\frac{2(L_{lk}+L_m)}{C_i}}\sin\frac{t-t_1}{\sqrt{2(L_{lk}+L_m)C_i}} \end{aligned} \tag{35}$$

This converter is mainly used in the high-input voltage medium or low power applications, so in (32) and (35), the latter terms are much smaller than the former terms. If the latter terms are ignored, the vary curves of V_{i1} and V_{i2} can be obtained in Fig.6 approximately. Generally, V_{i1} cannot be larger than V_i, So the resonances in Fig.6 can only occur in its first quarter period, and this limitation is shown in (36). It can be seen that the input voltage difference will increase as the turning on or off differences of the switches (ΔT_{on}, ΔT_{off}) increases.

$$\frac{T_{12}}{4}=\frac{\pi}{2}\sqrt{2(L_{lk}+L_m)C_i}>\Delta T_{on/off} \tag{36}$$

C. Design Principles of the Key Parameters

The input voltage differences of this converter cannot be avoid absolutely in the real conditions, so design principles of the key parameters are discussed here to reduce the input voltage differences.

From (23), (28) and Fig.5, it can be seen that for a constant duration from t_0 to t_1 (or from t_1 to t_2) and a constant difference between L_{m1} and L_{m2} (or L_{lk1} and L_{lk2}), the input voltage difference will decrease as the resonant periods (T_{i1}, T_{i2}) increase. From (32), (35) and Fig.6, it can be seen that if ΔT_{on} and ΔT_{off} are constant, the input voltage difference will decrease as the resonant period (T_{12}) increases. However, for this converter, the active IVS can be achieved both in the stages when all of the switches are turning on and off. Therefore, the suppression of the input voltage difference caused by the asynchronous operating of the switches should be mainly considered in the design process.

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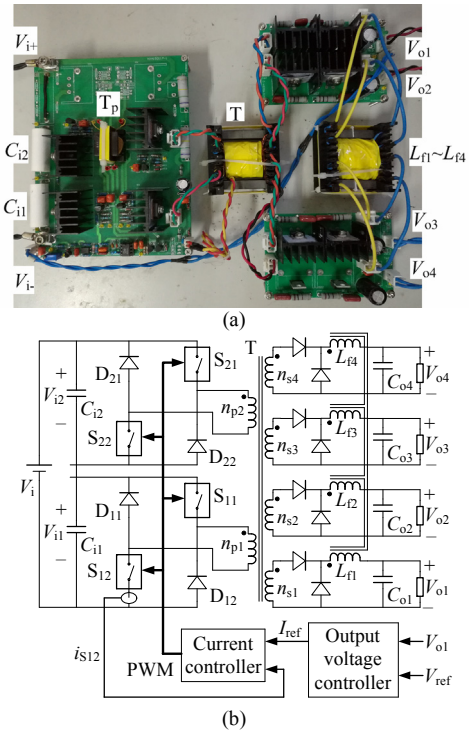

Fig.7. Photo and control scheme of the prototype. (a) Photo of the prototype. (b) The basic control scheme of the prototype.

Table I Experimental data

V_i/kV	1.0	1.1	1.2	1.3	1.4	1.5
V_{i1}/V	500	550	601	650	700	749
V_{i2}/V	501	550	600	651	700	750
η/% (P_o≈48W)	86.55	87.02	87.13	86.85	86.33	85.84
η/% (P_o=96W)	90.67	90.98	91.16	91.06	91.87	91.11

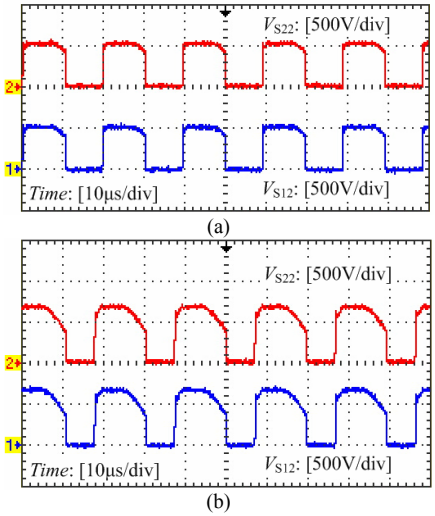

Fig.8. Voltage of S_{12} and S_{22}. (a) When V_i≈1060V. (b) When V_i≈1440V.

When the switches are turning on and off asynchronously in various series-modules, the maximum input voltage difference of this converter can be obtained from (32) and (35) approximately.

$$\begin{cases} \Delta V_{\text{i-on}} = V_{\text{i1}}(\Delta T_{\text{on}}) - V_{\text{i2}}(\Delta T_{\text{on}}) = V_{\text{i}}(1-\cos\dfrac{\Delta T_{\text{on}}}{\sqrt{2L_{\text{m}}C_{\text{i}}}}) \\ \Delta V_{\text{i-off}} = V_{\text{i1}}(\Delta T_{\text{off}}) - V_{\text{i2}}(\Delta T_{\text{off}}) = V_{\text{i}}(1-\cos\dfrac{\Delta T_{\text{off}}}{\sqrt{2L_{\text{m}}C_{\text{i}}}}) \end{cases} \quad (37)$$

where the latter terms in (32) and (35) are ignored in (37), and L_{lk} is much smaller than L_m, so it is also ignored.

If the input voltage difference is limited, for example, it is required that the maximum input voltage difference cannot be over than λV_i ($0<\lambda<1$), and then it can be obtained from (37) that:

$$L_{\text{m}}C_{\text{i}} \le \frac{\Delta T_{\text{on}}{}^2}{2[\arccos(1-\lambda)]^2}, \quad L_{\text{m}}C_{\text{i}} \le \frac{\Delta T_{\text{off}}{}^2}{2[\arccos(1-\lambda)]^2} \quad (38)$$

It can be seen that L_m and C_i are the key parameters, and for a limitation of the input voltage difference, there should be a minimum product value of L_mC_i. Generally, the value of L_m cannot be increased obviously due to the constant window area in the magnetic core of the transformer. Therefore, in the design process of this converter, for an almost constant value of L_m, the value of C_i can be increased appropriately to reduce the input voltage difference, and the calculation will be based on (38) to satisfy the specific design requirements.

IV. Experimental Verifications

To verify the proposed method and the theoretical analysis, a 96 W laboratory-made prototype of input-series two-transistor forward converter was built, as shown in Fig.7 (a), where the series-modules number N=2. This prototype is designed as an auxiliary power supply of the 1140Vdc frequency converter of a miner, the dc voltage of which will increase largely when the motor is operating in generating mode.

The basic control scheme of this prototype is shown in Fig.7 (b). A traditional peak current mode controller (UC3844) is adopted, the voltage and current signals V_{o1} and i_{S12} (current of S_{12}) are input to the controller, and a common pulse width modulation (PWM) signal is generated for the isolated driving circuits of S_{11}, S_{12}, S_{21} and S_{22}. In the driving circuits, a common pulse transformer T_p with one primary winding and four identical secondary windings is adopted, through which, four almost synchronous driving signals for S_{11}, S_{12}, S_{21} and S_{22} are generated. In the output circuits, a coupled-inductor is adopted instead of the four filter inductors (L_{f1}~L_{f4}), which is a conventional method to improve the multiple-output voltage cross-regulation feature in the forward converter, so it isn't discussed here.

The main circuit parameters and utilized components' type of this prototype are: 1) V_i: 1000-1500Vdc, 2) $V_{o1}=V_{o2}=V_{o3}=V_{o4}$=24V (n=4), I_{o1}=1.5A, $I_{o2}=I_{o3}$=1A, I_{o4}=0.5A, and P_{omax}=96W, 3) $C_{i1}=C_{i2}$=0.1μF, 4) S_{11}, S_{12}, S_{21}, S_{22}: K1271, the switching frequency is 50kHz, 5) the forward integrated-transformer T (ETD49): L_m=68.8mH, L_{lk}≈14μH, $n_{p1}=n_{p2}$=132, and $n_{s1}=n_{s2}=n_{s3}=n_{s4}$=14, 6) $L_{f1}=L_{f2}=L_{f3}=L_{f4}$=1mH (ETD49), and 7) $C_{o1}=C_{o2}=C_{o3}=C_{o4}$=1000μF.

Table I shows the input voltage of two series-modules and the efficiency of the prototype, where the input voltage results are measured by a dc voltmeter with the prototype operating under full load (P_o=96W). It can be seen that: the input voltage difference between the two serious-modules are very small, IVS of the prototype has been achieved efficiently, and it shows

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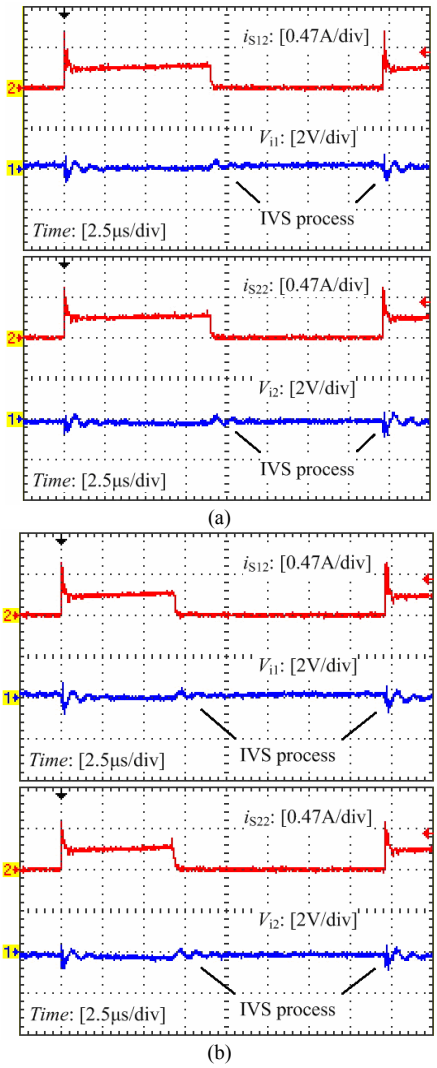

Fig.9. Input voltage of the two series-modules (ac coupling) and current of the switches S_{12} and S_{22}. (a) When V_i≈1060V. (b) When V_i≈1440V.

a good performance in conversion efficiency, which is similar to that of the conventional multiple-output two-transistor forward converter.

Fig.8 shows the voltage waveforms of S_{12} and S_{22} when V_i≈1060V and V_i≈1440V respectively. It can be seen that there are almost no differences between the two voltage waveforms and the voltage balancing of the switches in various series-modules has also been achieved in this prototype.

Fig.9 shows the input voltage waveforms of the two series-modules (ac coupling) and the current waveforms of the switches when V_i≈1060V and V_i≈1440V respectively, where the IVS processes in the two stages when the switches are turning on and off can be seen from the voltage waveforms. It can be seen that there are no obvious differences between the two current waveforms, and the key parameters are designed reasonably in this prototype.

Fig.10 shows the waveforms of V_{i1} (ac coupling) and i_{S12} when C_{i1}=C_{i2}=0.047μF and C_{i1}=C_{i2}=0.22μF respectively. Compared to the related results in Fig.8, it can be seen that the input voltage difference increases as the input filter capacitance

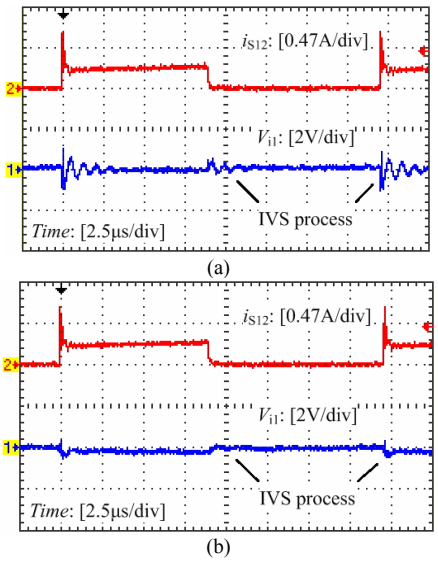

Fig.10. Waveforms of V_{i1} (ac coupling) and i_{S12} when the input filter capacitors are changed when V_i≈1060V. (a) C_{i1}=C_{i2}=0.047μF. (b) C_{i1}=C_{i2}=0.22μF.

decreases, and decreases as the input filter capacitance increases, which verifies the analysis in section III.

Fig.11 shows the input voltage waveforms of the two series-modules when V_i is changing. Fig.12 shows the input voltage waveforms of the two series-modules (ac coupling) to a stepped change of the output current I_{o1}. Because there is a bulk capacitor connected in parallel with the dc bus of the former equipment which is used to provide a high dc voltage (V_i) for this prototype, so V_i cannot be changed speedily, and it will also vary slightly with the load stepping. It can be seen that the changing process of the two input voltage are identical, and a good IVS performance has also been achieved in these two transient states. From the analysis in section II and the experimental results in Fig.9, it can be seen that the active IVS processes of this prototype are completed within the switching period, and cannot be affected in the transient states, which has also been verified here.

Fig.13 shows the waveforms of output voltage V_{o1}, V_{o2}, V_{o3} and V_{o4} to a stepped change of the output current I_{o1}. It can be seen that the coupled inductor method in the conventional forward converter is also suitable in this input-series converter prototype to improve the multiple-output voltage cross-regulation feature.

V. Conclusion

In this paper, aiming at the high-input voltage multiple-output applications, an input-series two-transistor forward converter is proposed and investigated. In this converter, a common forward integrated transformer is adopted, and all of the switches are operating synchronously. Firstly, the active IVS processes are analyzed both in the stage when the switches are turning on and in the stage when the switches are turning off. The analysis shows that when the input voltage difference appears, active IVS of this converter can be achieved by the coupling of primary windings of the forward integrated transformer, and IVS can be achieved more speedily as the equivalent leakage inductance of the forward integrated transformer decreases. Secondly, the input voltage differences

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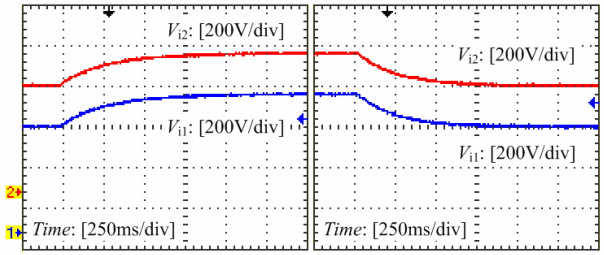

Fig.11. Input voltage of the two series-modules when V_i is changing.

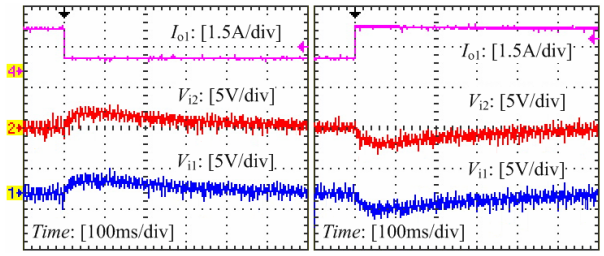

Fig.12. Input voltage of the two series-modules (ac coupling) to the stepped change of I_{o1}.

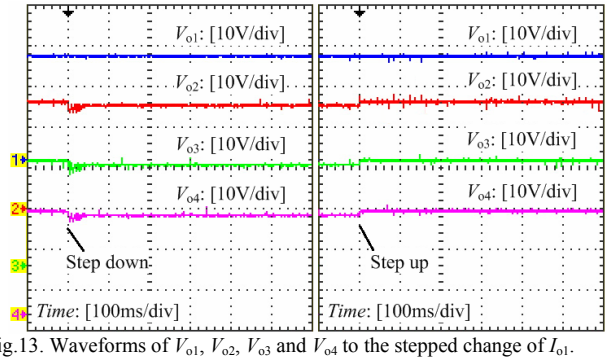

Fig.13. Waveforms of V_{o1}, V_{o2}, V_{o3} and V_{o4} to the stepped change of I_{o1}.

are discussed in the real conditions, and it shows that the input voltage differences will increase as the differences in various series-modules increase, which can be improved when the values of the equivalent excitation inductance and the input filter capacitor increase. Therefore, design principles of key parameters are obtained. Finally, the feasibility and validity of the proposed converter and the theoretical analysis are verified by the experimental results obtained from a 96W laboratory-made prototype.

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