High Voltage Gain Half-Bridge Z-Source Inverter with Low Voltage Stress on Capacitors

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***Abstract*—In this paper, a new topology for half-bridge Z-source inverter (HB-ZSI) is proposed. The proposed topology has only one impedance network. Unlike to the conventional half-bridge inverter, the proposed topology can provide zero voltage level at the output. It also increases output voltage level and stabilizes it in the desired value. Capacitor voltage stress in the proposed topology is low and therefore nominal voltage of capacitor and cost decreases. In this paper, the steady state analysis of the proposed inverter in two new operations which are named synchronous operation of diodes (SOD) and asynchronous operation of diodes (AOD) is conducted based on mathematics calculations. A method to obtain high voltage gains by cascading the Z-network and combining middle inductors is presented that leads to cost, size and weight reduction. Comparison among the proposed converter with conventional ones shows its excellent performance. The experimental results have good agreement with analytical analysis for the proposed topology.**

***Index Terms*—Half-bridge inverter, Z-source inverter, shoot through (ST), high voltage gain converter.**

I. Introduction

THE Z-source inverter (ZSI) has been presented in [1]. In Z-source inverter, capacitors' voltage stress is high, therefore in [2], quasi Z-source inverter (QZSI) has been presented to solve this problem. In [3], switched inductor Z-source inverter (SL-ZSI) has been introduced to obtain high voltage gains. Its main disadvantage is the increasing capacitors' voltage stress in comparison with the conventional ZSI and QZSI. In [4], a new topology called switched boost inverter (SBI) has been presented that its disadvantage is lower voltage gain in comparison with the conventional ZSI. In [5], a new topology called current-fed switched inverter (CFSI) has been introduced to enhance characteristics of the presented SBI in [4]. To overcome the inrush current problems at start-up, capacitor voltage stress and obtaining high voltage gains, a topology called L-ZSI has been presented in [6]. Applying Z-source concept into half-bridge converters results in Z-source half-bridge converters [7-10]. In [7], the presented topology has two impedance networks. In [8], for industrial applications such as electroplating and electrochemical, the Z-source half-bridge converter has been presented, in which, instead of putting two impedance networks, only one impedance network is required. In half-bridge Z-source inverter (HB-ZSI) with one impedance network, capacitors' voltage stress is high and the output voltage waveform has one positive level and one negative level that limit the applications. In [9], a quasi-Z-source half-bridge galvanically isolated dc/dc converter has been presented. The topology could be envisioned as an alternative to the boost half-bridge dc-dc converter but the benefit of its symmetric structure reduces the threat of transformer saturation due to the dc flux. In [10], the half-bridge impedance source converter has been simplified by the implementation of the asymmetrical half-bridge concept. However, the asymmetrical half-bridge topology has only on ST state per switching period; so, its passive elements have large values. In [11], based on provided cascading method in [12] the full-bridge step-up dc/dc converter with cascaded quasi-Z-source networks has been presented. The presented cascaded QZSI has voltage boost and buck functions in a single stage, continuous input current, and improved reliability. In [13], the developed topology for switched-Z-source inverter based on cascaded switched-inductors cells has been presented. Although developed topology has high voltage gain but voltage stress on capacitor is high. In [14], a topology for half-bridge switched boost inverter based on [4] has been presented. This inverter uses more active elements rather than capacitors and inductors. By using more active elements, switching losses can reduce efficiency.

In this paper, a new topology for half-bridge Z-source inverter is proposed. In upcoming sections, first the proposed topology is introduced then different operating modes are analyzed and the critical inductances between SOD and AOD are calculated. Also extension of the proposed topology is discussed to obtain higher voltage gains. Comparison of proposed converter with conventional topologies is also provided. In the last section, the correctness operation of the proposed topology is validated by experimental results.

II. Proposed Topology

Fig. 1 shows the power circuit of the proposed inverter with one impedance network. According to this figure, the proposed half-bridge converter consists of inductors L_1 and

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L_2, capacitors C_1 and C_2, diodes D_a and D_b, switches S_1 and S_2, output load and two dc voltage sources with amplitude of V_i. The proposed topology can be used in electroplating [8]. Also, the proposed inverter can be used in a galvanically isolated dc/dc conversion [15].

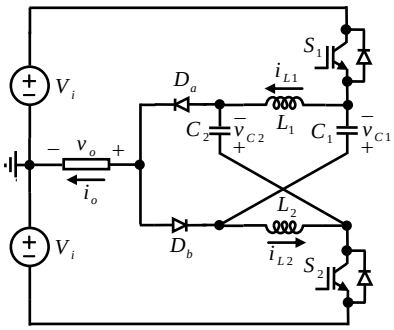

Fig. 1. Power circuit of the proposed topology.

A. Operating Modes of the Proposed Inverter in SOD

The operating modes of the proposed inverter in SOD are analyzed in this sub- section. Load type is considered resistive. In SOD, the diodes are turned on and turned off simultaneously. In this study, D_{S1} and D_{S2} are the duty cycles of switches S_1 and S_2, respectively and D_{ST} is the division result of turn on time period for S_1 and S_2 simultaneously to the total switching period. It is to be mentioned that control method of the proposed inverter is based on presented control method in [16], so, turn on moments for S_1 and S_2 have phase difference of 180 together and the following equations are obtained:

$$D_{S1} = D_{S2} = D \tag{1}$$

$$D = 0.5(1 + D_{ST}) \tag{2}$$

Also according to symmetry in Fig. 1, we can write:

$$i_{L1} = i_{L2} = i_L \tag{3}$$

$$v_{L1} = v_{L2} = v_L \tag{4}$$

$$V_{C1} = V_{C2} = V_C \tag{5}$$

where i_{L1} and i_{L2} are the inductors L_1 and L_2 currents, respectively that are shown as i_L. v_{L1} and v_{L2} are the inductors L_1 and L_2 voltages, respectively and are shown as v_L. Also V_{C1} and V_{C2} are the capacitors C_1 and C_2 average voltages, respectively that are shown as V_C.

1) First Operating Mode ($0 \le t < 0.5D_{ST}T_s$):

In this operating mode both of S_1 and S_2 switches are on and diodes D_a and D_b are off. In this time interval, the inductors' voltage is positive; so, their current reaches from a minimum value (I_{LV}) to a maximum value (I_{LP}). Also the stored energy in capacitors and their voltage are decreased. By using Kirchhoff's voltage law (KVL), we can write:

$$v_L = 2V_i + V_C \tag{6}$$

$$v_{Da} = v_{Db} = -V_i - V_C \tag{7}$$

where v_{Da} and v_{Db} are the voltages of diodes D_a and D_b, respectively that are assumed negative. Because diodes D_a and D_b are off, the load voltage (v_o) in this operating mode becomes zero and we have:

$$v_o = 0 \tag{8}$$

Hence, the proposed half-bridge inverter unlike to the conventional one can provide zero voltage level in the output.

2) Second Operating Mode ($0.5D_{ST}T_s \le t < 0.5T_s$):

In this operating mode the switches S_1 and S_2 are on and off, respectively and both D_a and D_b are on. Therefore the output voltage will be positive and the voltage of capacitors C_1 and C_2 will be decrease and increase, respectively. Also, due to the negative voltage across inductors, their current decreases from a maximum value (I_{LP}) to a minimum value (I_{LV}). By applying KVL, we can write:

$$v_L = -V_C \tag{9}$$

$$v_o = v_{o,\max} = V_i + V_C \tag{10}$$

3) Third Operating Mode ($0.5T_s \le t < 0.5(1 + D_{ST})T_s$):

The operating mode in the time interval $0.5T_s \le t < 0.5(1 + D_{ST})T_s$ is similar to the mentioned first mode.

4) Fourth Operating Mode ($0.5(1 + D_{ST})T_s \le t < T_s$):

In this operating mode the switches S_1 and S_2 are off and on, respectively and both D_a and D_b are on. Therefore the output voltage is negative and the energy of capacitors C_2 and C_1 will decrease and increase, respectively. Similar to the previous operating mode, the inductor's current decreases with slope $-V_C / L$ that leads to a decrement in its energy. The voltage across inductor is the same as (9) and by applying KVL, the following equation is obtained:

$$v_o = v_{o,\min} = -V_i - V_C \tag{11}$$

Based on the previous discussions the voltage across inductors is positive when both S_1 and S_2 are on and otherwise the voltage is negative. Considering the voltage balance law in inductors and by using (6) and (9) the capacitor average voltage is calculated as follows:

$$V_C = \frac{2 - 4D}{4D - 3} V_i \tag{12}$$

By replacing the D value from (2), the above equation is rewritten as follows:

$$V_C = \frac{2D_{ST}}{1 - 2D_{ST}} V_i \tag{13}$$

In above equation, the theoretical value of D_{ST} is in interval $0 < D_{ST} < 0.5$.

Using (10) to (12), the maximum output voltage is calculated as follows:

$$v_{o,\max} = -v_{o,\min} = \frac{1}{3 - 4D} V_i \tag{14}$$

By replacing the D value from (2), the above equation is rewritten as follows:

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$$v_{o,\max} = -v_{o,\min} = \frac{1}{1-2D_{ST}} V_i = BV_i \quad (15)$$

Boost factor (B) in above equation, is the ratio of maximum output voltage to the value of one of the input voltage sources. Fig. 2(a) shows the main waveforms of the proposed inverter in SOD. In this figure, G_{S1} and G_{S2} are the trigger pulses to the switches S_1 and S_2, respectively. 1 and 0 are the on and off states of switches, respectively.

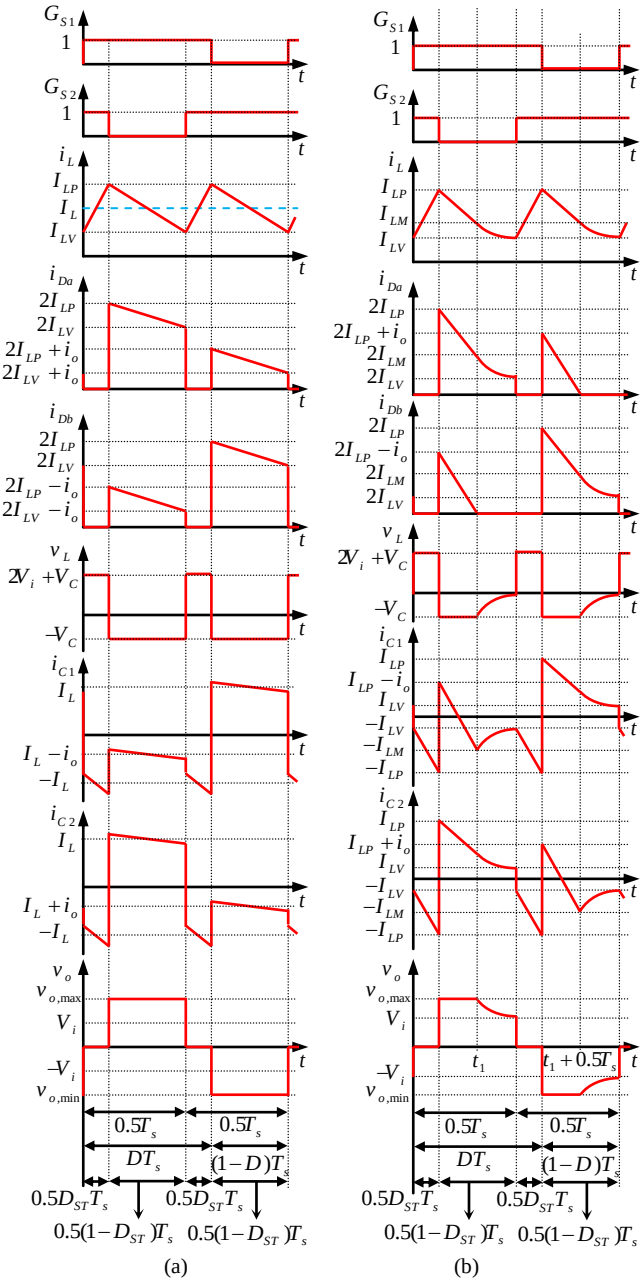


Fig. 2. The voltage and current waveforms of the proposed topology; (a) in SOD; (b) in AOD.

B. Operating Modes of the Proposed Inverter in AOD

The AOD is achieved, if any of the inductance values of inductors, output load, switching frequency or ST duty cycle is selected in such a way that the current through diode D_a in time interval $0.5(1+D_{ST})T_s \le t < T_s$ and the current through diode D_b in time interval $0.5D_{ST}T_s \le t < 0.5T_s$ are become zero. In next sub-sections, the different operating in AOD is explained.

1) First Operating Mode:

In this operating mode both S_1 and S_2 are on and diodes D_a and D_b are off. The inductors' voltage is positive so their current reaches from a minimum value (I_{LV}) to a maximum value (I_{LP}). By applying Kirchhoff's current law (KCL), we can write:

$$i_{C1} = -i_{L2} = -i_L \quad (16)$$

$$i_{C2} = -i_{L1} = -i_L \quad (17)$$

Also, the equations (6)-(8) are correct in this operating mode.

2) Second Operating Mode:

In this operating mode the switches S_1 and S_2 are on and off, respectively. Also, the diodes D_a and D_b are on. Sum of the currents through inductors L_1 and L_2 flow through diode D_a. The current through diode D_b is calculated as follows:

$$i_{Db} = i_{L1} + i_{L2} - i_o = 2i_L - i_o \quad (18)$$

The equations (9) and (10) are true for this operating mode; so, the currents through L_1 and L_2 decrease linearly from I_{LP} to I_{LM} at the end of this operating mode ($t = t_1$) and the output voltage will be positive. By applying KCL, the following equations are derived:

$$i_{C1} = i_{L1} - i_o = i_L - i_o \quad (19)$$

$$i_{C2} = i_{L2} = i_L \quad (20)$$

It is noticeable that at the end of this operating mode, the current through diode D_b is zero.

3) Third Operating Mode:

In this operating mode the switches S_1 and S_2 are on and off, respectively. Also, operation of diodes is asynchronous and the diodes D_a and D_b are on and off, respectively. Like the second operating mode, sum of the currents through inductors L_1 and L_2 flow through diode D_a. For inductors L_1 and L_2, by considering the new base time, the following equations are calculated:

$$i_L = \frac{V_i}{2R_L} + \left(\frac{V_i + V_C}{2R_L} - \frac{V_i}{2R_L} \right) e^{-\frac{2R_L}{L}t} \quad (21)$$

The above equation shows that current through inductors decreases exponentially.

$$v_L = -V_C e^{-\frac{2R_L}{L}t} \quad (22)$$

The above equation shows that voltage across inductors increases exponentially. By applying KVL and using (22), the output voltage is calculated as follows:

$$v_o = V_i + V_C e^{-\frac{2R_L}{L}t} \quad (23)$$

The equation (23) shows that value of output voltage is not constant.

4) Fourth Operating Mode:

The fourth operating mode is similar to the mentioned first operating mode.

5) Fifth Operating Mode:

In this operating mode the switches S_1 and S_2 are off and on, respectively. Also, the diodes D_a and D_b are on. Sum of the currents through inductors L_1 and L_2 flow through diode D_b. The current through diode D_a is calculated as follows:

$$i_{Da} = i_{L1} + i_{L2} + i_o = 2i_L + i_o \quad (24)$$

The equations (9) and (11) are true for this operating mode; so, the currents through L_1 and L_2 decrease linearly from I_{LP} to I_{LM} at the end of this operating mode ($t = t_1 + 0.5T_s$) and the output voltage will be negative. By applying KCL, the following equations are derived:

$$i_{C1} = i_{L1} = i_L \quad (25)$$

$$i_{C2} = i_{L2} + i_o = i_L + i_o \quad (26)$$

It is noticeable that at the end of this operating mode, the current through diode D_a is zero.

6) Sixth Operating Mode:

In this operating mode the switches S_1 and S_2 are off and on, respectively. Also, operation of diodes is asynchronous and the diodes D_a and D_b are off and on, respectively. Like the fifth operating mode, sum of the currents through inductors L_1 and L_2 flow through diode D_b. For inductors L_1 and L_2, by considering the new base time, the equations (21) and (22) are true. By applying KVL and using (22), the output voltage is calculated as follows:

$$v_o = -V_i - V_C e^{-\frac{2R_L}{L}t} \quad (27)$$

Equations (23) and (27) show that output voltage waveform in AOD changes exponentially; so, the symmetry of waveform is destroyed and the proper selection of inductance for not entering into AOD is necessary. Fig. 2(b) shows the main waveforms of the proposed inverter in AOD. In next sub-section, the critical inductances between SOD and AOD are calculated.

C. Calculating Critical Inductance between SOD and AOD

According to Fig. 3, in boundary operation between SOD and AOD, the current through diode D_a at the end of time interval $0.5(1+D_{ST})T_s \le t \le T_s$ and the current through diode D_b at the end of time interval $0.5D_{ST}T_s \le t \le 0.5T_s$ are become zero; so, using Figs. 2 and 3, the following equation can be written for the current through diode D_a in $t = T_s$:

$$i_{Da}(t = T_s) = 2I_{LV} + i_o = 0 \quad (28)$$

Also, the following equation can be written for the current through diode D_b in $t = 0.5T_s$:

$$i_{Db}(t = 0.5T_s) = 2I_{LV} - i_o \quad (29)$$

By using the integral of C_1 or C_2 current that is zero in one switching period, critical inductances between SOD and AOD are calculated from (15), (28) and (29) as follows:

$$L_{1,\min} = L_{2,\min} = L_{\min} = (1-D_{ST})(1-2D_{ST})\frac{R_L}{f_s} \quad (30)$$

Fig. 4 shows normalized critical inductance as a function of D_{ST} at the SOD/AOD boundary.

D. Design Considerations

In AOD, the symmetry of output waveform is destroyed but in SOD, the output voltage waveform is completely symmetric and the proposed inverter has a better performance; so, design considerations are derived just for SOD. Calculations of inductors' current ripple and capacitors' voltage ripple are important factors to design the proper values for inductor and capacitor. First by using equation $v_L = L(di_L/dt)$, (9) and (13) the value of inductors' current ripple is calculated as follows:

$$|\Delta i_L| = \frac{D_{ST}(1-D_{ST})T_s}{L(1-2D_{ST})}V_i \quad (31)$$

According to the second operating mode in SOD and assuming that inductors' current ripple is negligible, the following equation is obtained for the currents through capacitors C_1 and C_2:

$$i_{C1} = i_{C2} = I_L \quad (32)$$

In above equation, I_L is the inductors' average current.

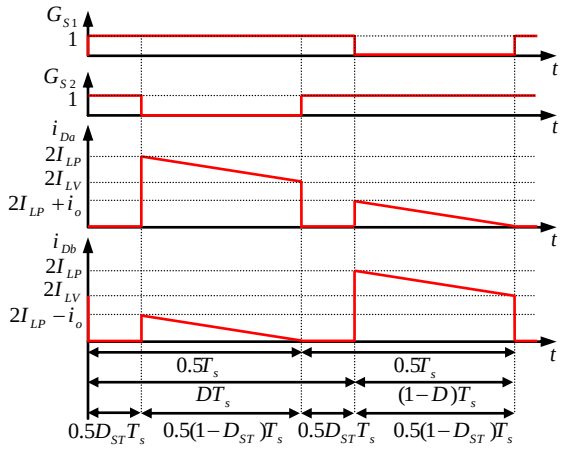


Fig. 3. The currents through diodes D_a and D_b in boundary operation between SOD and AOD.

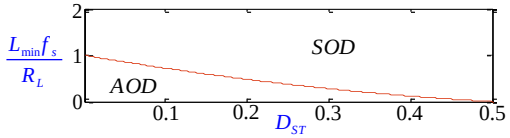


Fig. 4. Normalized $L_{\min}$ versus D_{ST} at the SOD/AOD boundary.

Using (2), (32) and equation $i_{C2} = C_2(dv_{C2}/dt)$, the voltage ripple of capacitors is calculated as follows:

$$|\Delta v_C| = \frac{(1-D_{ST})T_s}{2C}I_L \quad (33)$$

Above equation shows the important role of I_L in calculation of capacitors' voltage ripple. By considering the current balance law in capacitors, the value of I_L is calculated as follows:

$$I_L = \frac{1-D_{ST}}{2R_L(1-2D_{ST})^2}V_i \quad (34)$$

where R_L is the value of output resistive load.

By replacing I_L from above equation in (33), $|\Delta v_C|$ is obtained as follows:

$$|\Delta v_C| = \frac{(1-D_{ST})^2}{4R_L C f_s (1-2D_{ST})^2} V_i \quad (35)$$

The voltage and current stress values are necessary factors in proper switch selection especially for practical circuits. By applying KCL and using (3) we have:

$$i_{S1} = i_{S2} = i_{L1} + i_{L2} = 2i_L \quad (36)$$

According to the above equation, the maximum value for switch current $(i_{S1,\max}, i_{S2,\max})$ happens when inductors' current is in its maximum value. By using (31) and (34) we can write:

$$i_{S1,\max} = i_{S2,\max} = \frac{(1-D_{ST})[L + R_L D_{ST}(1-2D_{ST})T_s]}{R_L L (1-2D_{ST})^2} V_i \quad (37)$$

For calculation of maximum voltage stress on S_1 $(v_{S1,\max})$ and S_2 $(v_{S2,\max})$, KVL is applied and by using (14) we can write:

$$v_{S1,\max} = v_{S2,\max} = v_{S,\max} = 2(V_i + V_C) = \frac{2}{1-2D_{ST}} V_i \quad (38)$$

In SOD, for determining appropriate values for capacitors used in proposed converter (Fig. 1), we may use allowable voltage ripple range, $x_C\%$, which defined as:

$$x_C\% = \frac{|\Delta v_C|}{V_C} \quad (39)$$

Replacing values of $|\Delta v_C|$ and V_C from (35) and (13) in above equation, the rated value of capacitance according to allowable voltage ripple range is defined as:

$$C = \frac{(1-D_{ST})^2}{8R_L f_s D_{ST}(1-2D_{ST}) x_C\%} \quad (40)$$

By same way, by considering current ripple, the appropriate values of inductances can be calculated. Range of allowable current ripple, $x_L\%$, is defined as follows:

$$x_L\% = \frac{|\Delta i_L|}{I_L} \quad (41)$$

Replacing the values of I_L and $|\Delta i_L|$ from (34) and (31) in above equation, the rated value of inductances can be calculated as follows:

$$L = \frac{2R_L D_{ST}(1-2D_{ST})}{f_s x_L\%} \quad (42)$$

III. Extension of the Proposed Topology

In this section, extension of the proposed topology is presented. Fig. 5(a) shows the extension of the proposed topology with three cascaded Z-networks.

Fig. 5(b) shows the extension of the proposed inverter with N Z-networks in which N is odd to keep symmetry and obtaining desired characteristics. As there are two inductors in conventional Z-source network, it is expected that there be $2N$ inductors in extension of the proposed topology with N Z-network but because of merging middle inductors only use $N+1$ inductors, which leads to the implementation of $N-1$ less inductors. Considering the symmetry in Fig. 5(b), in SOD the following equations are obtained:

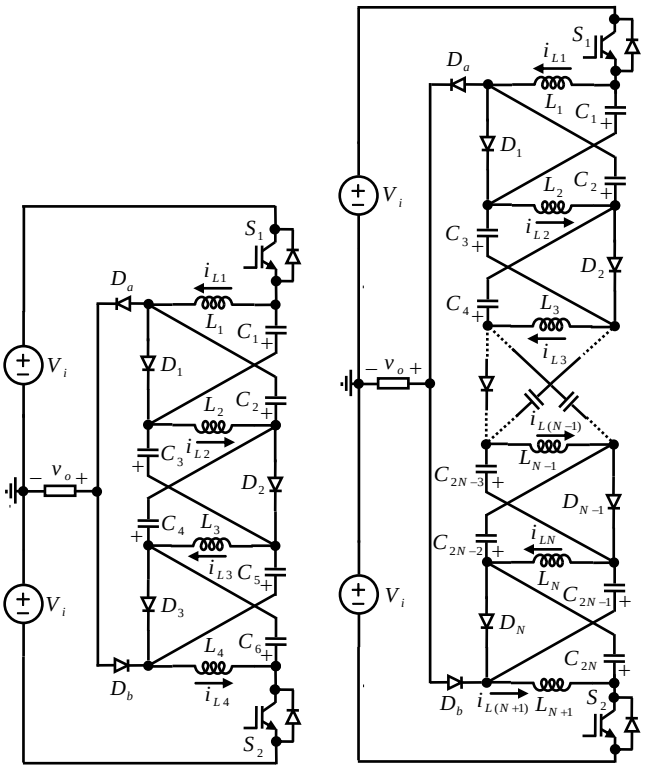
$$i_{L1} = i_{L(N+1)} \quad (43)$$

$$i_{L2} = i_{L3} = \cdots = i_{L(N-1)} = i_{LN} \quad (44)$$

$$V_{C1} = V_{C2} = \cdots = V_{C(2N-1)} = V_{C2N} = V_C = \frac{2D_{ST}}{1-(N+1)D_{ST}} V_i \quad (45)$$

$$v_{o,\max} = -v_{o,\min} = \frac{1-(N-1)D_{ST}}{1-(N+1)D_{ST}} V_i = BV_i \quad (46)$$

In SOD, on and off states of power semiconductors in different operating modes and other related equations are summarized in Table I.



(a) (b)

Fig. 5. Extension of the proposed topology; (a) with three Z-networks; (b) with N Z-networks.

TABLE I
ON AND OFF STATES OF POWER SEMICONDUCTORS AND OTHER RELATED EQUATIONS

	First and third operating modes	Second operating mode	Fourth operating mode
S_1	On	on	off
S_2	On	off	on
D_a	off	On	off
D_b	off	Off	on
$D_1, D_2, \cdots, D_N$	off	On	on
v_{Da}	$-V_i - NV_C$	0	$-(N-1)V_C$
v_{Db}	$-V_i - NV_C$	$-(N-1)V_C$	0
$v_{D1} = \cdots = v_{DN}$	$-2V_i - (N+1)V_C$	0	0
v_L	$2V_i + NV_C$	$-V_C$	$-V_C$
v_o	0	$V_i + V_C$	$-V_i - V_C$

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IV. Comparison of The Proposed and Conventional Inverters

A. Comparison of Boost Factor and Voltage Stress on Capacitors

As mentioned before, by increasing the number of Z-networks and ST duty cycle, the voltage gain is increased. Figs. 6(a) and 6(b) compares the boost factor of the proposed topology with the conventional inverters in the case of $N=1$ and $N>1$, respectively. According to these figures, by setting the number of cascaded networks in different duty cycle values, we can obtain higher boost factor in comparison with the topologies in [1-8].

Figs. 6(c) and 6(d) shows the comparison results of voltage stress on capacitors between the proposed and conventional inverters in the case of $N=1$ and $N>1$, respectively. According to these figures, the capacitors voltage stresses in the proposed inverter are much lower than the presented topologies in [1], [3-5] and [7] which has various advantages such as reduced cost due to low rated values of capacitors.

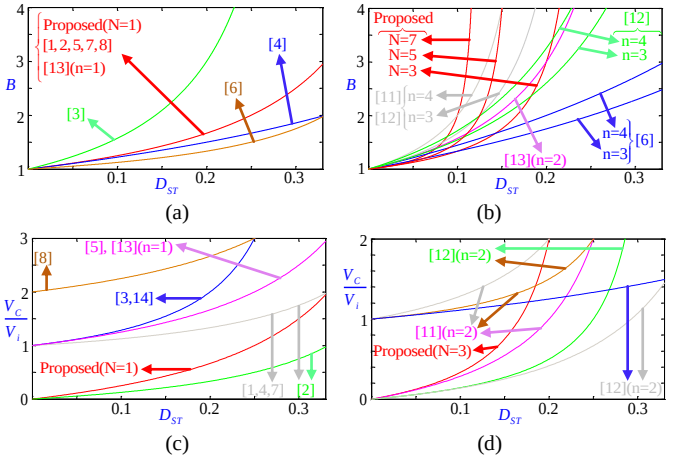

Fig. 6. Comparison of the proposed and conventional inverters; (a) in terms of boost factor ($N=1$); (b) in terms of boost factor ($N>1$); (c) in terms of capacitors voltages stresses ($N=1$); (d) in terms of capacitors voltages stresses ($N>1$).

B. Comparison of the Harmonics Amplitude of Output Voltage

Considering Fig. 2(a), for the proposed inverter the Fourier series of output voltage waveform is calculated by the following equation:

$$v_o(t)=\sum_{n\ \text{odd}} V_n \sin(n\omega t) \tag{47}$$

Due to the half-wave symmetry, V_n is calculated as follows:

$$V_n=\frac{4v_{o,\max}}{n\pi}\cos(0.5n\pi D_{ST}) \tag{48}$$

By using (15) and (48), the RMS value of fundamental harmonic ($V_{1,RMS}$) is calculated as follows:

$$V_{1,RMS}=\frac{4\cos(0.5\pi D_{ST})}{\pi\sqrt{2}(1-2D_{ST})}V_i \tag{49}$$

By using (46) and (48), the RMS value of fundamental harmonic ($V_{1,RMS}$) for the extended proposed topology is calculated as follows:

$$V_{1,RMS}=\frac{4[1-(N-1)D_{ST}]\cos(0.5\pi D_{ST})}{\pi\sqrt{2}[1-(N+1)D_{ST}]}V_i \tag{50}$$

In the classical half-bridge inverter, the RMS value of fundamental harmonic ($V_{1,RMS}$) is calculated as follows:

$$V_{1,RMS}=\frac{4V_i}{\pi\sqrt{2}} \tag{51}$$

Fig. 7 shows the comparison between the proposed and classical half-bridge inverters as regard to the RMS value of fundamental harmonic of the output voltage. According to this figure, by increasing ST duty cycle, the RMS value of fundamental harmonic is increased, so, proposed inverter has better situation rather than the classical half-bridge inverter.

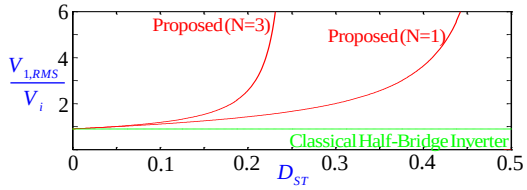

Fig. 7. Comparison between the proposed and classical half-bridge inverters as regard to the RMS value of fundamental harmonic of the output voltage.

V. Experimental Results

In this section, the correct operation of the basic proposed topology with $N=1$ is validated by experimental results. Selective values of elements and variables are summarized in Table II.

TABLE II
SELECTIVE VALUES

V_i	L	C	x_L%	x_C%	R_L	f_s	D	D_{ST}
20V	775μH	470μF	45.4%	0.96%	14.66Ω	10kHz	0.6	0.2

The critical inductance between SOD and AOD is calculated $705\mu H$ from (30). The used inductor maintains the proposed inverter in SOD. Power MOSFET IRF840 and diode MUR1560G are used. Fig. 8 shows experimental results obtained for the proposed inverter with $N=1$. Fig. 8(a) shows applied signals to power MOSFETs S_1 and S_2 gates based on presented control method in [16]. Fig. 8(b) shows current through L_1, which has average value of 1.50A. This value is consistent with value 1.51A from (34). The voltage across this inductor is shown in Fig. 8(c). According to this figure, when S_1 and S_2 switches are on simultaneously, the inductors voltages are positive and equal to 50V, otherwise they are negative and equal to -12V. All of these results coincide with values 53.33V and -13.33V obtained from (6) and (9). Fig. 8(d) shows voltage across capacitor C_1. According to this figure, capacitor average voltage value is almost 12V. This value corresponded to the value 13.33V obtained from (13). Waveform of current through this capacitor is shown in Fig. 8(e). As expected this waveform obeys capacitor current balance law and coincides with

previous analysis. Fig. 8(f) shows the waveform of output voltage. According to this figure, this converter converted DC 20V to AC voltage with approximate maximum and minimum value +31V and -31V. These results coincide with values obtained from (8) and (15), 33.33V and -33.33V.

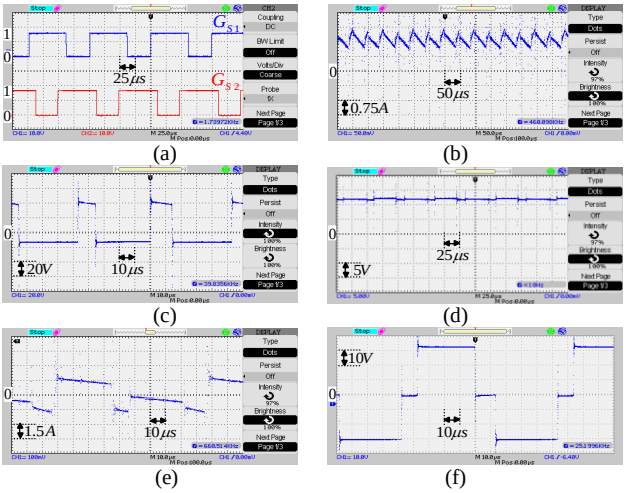

Fig. 8. Key waveforms for $N=1$ in SOD; (a) Trigger pulses; (b) i_{L1}; (c) v_{L1}; (d) v_{C1}; (e) i_{C1}; (f) Output load voltage.

VI. Conclusion

In this paper, a new topology for Z-source half-bridge inverter is proposed and its various operating modes were studied. Also, critical inductances between SOD and AOD were calculated. The equations of voltage and current of all elements and also voltage gain of the proposed inverter were calculated. Approach to reach high voltage gain through the series Z-networks and merging middle inductors which lead to less cost and weight were presented. Comparison results of the proposed inverter with various conventional inverters in terms of voltage gain and stress across capacitors prove its advantages. The proposed inverter against conventional half-bridge topology can produce zero voltage level at output, too. Compatibility of results from experimental with the results extracted from theoretical calculation confirms the accuracy of content provided.

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