S3 Technologies

IEEE Dot Net | Java | Embedded | Image Processing | Android | Networking |VLSI |Application Projects

IEEE 2016-2017 VLSI PROJECTS

S.NO	Titles	YEAR
S3001	Analysis and Mapping for Thermal and Energy Efficiency of 3-D Video Processingon 3- D Multicore Processors	2016
S3002	5-bit 5-GS/s Non interleaved Time-Based ADC in 65-nm CMOS for Radio-Astronomy Applications M (IEEE 2016)	2016
S3003	Design Methodology for Voltage-Scaled Clock Distribution Networks	2016
S3004	A Low-Voltage Radiation-Hardened 13T SRAM Bitcell for Ultralow Power Space Applications	2016
S3005	A 28-nm CMOS 1 V 3.5 GS/s 6-bit DAC With Signal-Independent Delta-I Noise DfT Scheme	2016
S3006	A Calibration Technique for Bang-Bang ADPLLs Using Jitter Distribution Monitoring	2016
S3007	A Compact One-Pin Mode Transition Circuit for Clock Synchronization in Current Mode Controlled Switching Regulators	2016
S3008	A Fine-Grained Control Flow Integrity Approach Against Runtime Memory Attacks for Embedded Systems	2016
S3009	A Low-Voltage Radiation-Hardened 13T SRAM Bit cell for Ultralow Power Space Applications	2016
S3010	A VLSI Circuit Emulation of Chemical Synaptic Transmission Dynamics and Postsynaptic DNA Transcription	2016
S3011	Area-Delay Efficient Digit-Serial Multiplier Based on k-Partitioning Scheme Combined With TMVP Block Recombination Approach	2016
S3012	Design Methodology for Voltage-Scaled Clock Distribution Networks	2016
S3013	Detector for MLC NAND Flash Memory Using Neighbor-A-Priori Information	2016
S3014	Enhanced Built-In Self-Repair Techniques for Improving Fabrication Yield and Reliability of Embedded Memories	2016
S3015	Fault Tolerant Parallel Filters Based on Error Correction Codes	2016
S3016	Improving Convergence and Simulation Time of Quantum Hydrodynamic Simulation Application to Extraction of Best 10-nm Fin FET Parameter	2016

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	Values	
S3017	Optimum pMOS-to-nMOS Width Ratio for Efficient Subthreshold CMOS Circuits	2016
S3018	Utilization-Aware Self-Tuning Design for TLC Flash Storage Devices	2016
S3019	A Modified Partial Product Generator for Redundant Binary Multipliers	2016
S3020	A New Paradigm of Common Sub expression Elimination by Unification of Addition and Subtraction	2016
S3021	Design-Efficient Approximate Multiplication Circuits Through Partial Product Perforation	2016
S3022	High-Performance Pipelined Architecture of Elliptic Curve Scalar Multiplication Over GF(2m)	2016
S3023	A Scalable Approximate DCT Architectures for Efficient HEVC Compliant Video Coding	
S3024	Design for Testability of Sleep Convention Logic	2016
S3025	Floating-Point Butterfly Architecture Based on Binary Signed-Digit Representation	2016
S3026	A Low-Cost Low-Power Ring Oscillator-based Truly Random Number Generator for Encryption on Smart Cards	2016
S3027	A New Fast and Area-Efficient Adder-Based Sign Detector for RNS {2n- 1, 2n, 2n+ 1}	2016
S3028	A 1–16-Gb/s All-Digital Clock and Data Recovery With a Wideband, High-Linearity Phase Interpolator.	2016
S3029	Multiplier less Unity-Gain SDF FFTs	2016
S3030	A High-Throughput Energy-Efficient Implementation of Successive Cancellation Decoder for Polar Codes Using Combinational Logic	2016
S3031	Low-Power Variation-Tolerant Nonvolatile Lookup Table Design	2016

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S3032	Thermal-Aware Small-Delay Defect Testing in Integrated Circuits for Mitigating Overkil	2016
S3033	A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications	2016
S3034	Input-Based Dynamic Reconfiguration of Approximate Arithmetic Units for Video Encoding	2016
S3035	High-Throughput Finite Field Multipliers Using Redundant Basis for FPGA and ASIC Implementations	2016
S3036	Accelerated Accurate Timing Yield Estimation Based on Control Variates and Importance Sampling	2016