VLSI TITLES FOR 2015-16

S.NO	TITLE	DOMAIN	YEAR
1	Area-EfficientFixed-WidthSquarerwith Dynamic Error-Compensation Circuit	Area Efficient	2015
2	Reverse Converter Design via Parallel-Prefix Adders: Novel Components, Methodology, and Implementations	Area Efficient	2015
3	A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications	Area Efficient	2015
4	An Area-Efficient Relaxed Half-Stochastic Decoding Architecture for Non-binary LDPC Codes	Area Efficient	2015
5	Area-Delay-Power Efficient Fixed-Point LMS Adaptive Filter With Low Adaptation-Delay	Area Efficient	2014
6	Improved 8-Point Approximate DCT for Image and Video Compression Requiring Only 14 Additions	Area Efficient	2014
7	An Optimized Modified Booth Recoder for Efficient Design of the Add-Multiply Operator	Area Efficient	2014
8	High-Throughput Finite Field Multipliers Using Redundant Basis for FPGA and ASIC Implementations	High Speed	2014
9	A 5.8-GHz Wideband TSPC Divide-by-16/17 Dual Modulus Prescaler	High Speed	2015

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10	An Accuracy-Adjustment Fixed-Width Booth Multiplier Based on Multilevel Conditional Probability	High Speed	2015
11	Fast Sign Detection Algorithm for the RNS Moduli Set $\{2n+1-1, 2n-1, 2n\}$	High Speed	2015
12	Low-Cost High-Performance VLSI Architecture for Montgomery Modular Multiplication	High Speed	2015
13	High-Throughput Multi standard Transform Core Supporting MPEG/H.264/VC-1 Using Common Sharing Distributed Arithmetic	High Speed	2015
14	Area–Delay–Power Efficient Carry-Select Adder	High Speed	2014
15	Critical-Path Analysis and Low-Complexity Implementation of the LMS Adaptive Algorithm	High Speed	2014
16	A Low-Power Hybrid RO PUF With Improved Thermal Stability for Lightweight Applications	Low Power	2015
17	Low-Power and Area-Efficient Shift Register Using Pulsed Latches	Low Power	2015
18	Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic	Low Power	2015
19	Energy-Efficient Approximate Multiplication for Digital Signal Processing and Classification Applications	Low Power	2015
20	Wear out Resilience in NoCs Through an Aging Aware Adaptive Routing Algorithm	Low Power	2015
21	Low-Power Programmable PRPG With Test	Low Power	2014

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	Compression Capabilities		
22	Data encoding techniques for reducing energy Consumption in network-on-chip	Low Power	2015
23	In-Field Test for Permanent Faults in FIFO Buffers of NoC Routers	Testing	2015
24	Recursive Approach to the Design of a Parallel Self-Timed Adder	Testing	2015
25	Input Vector Monitoring Concurrent BIST Architecture Using SRAM Cells	Testing	2014
26	Efficient Coding Schemes for Fault-Tolerant Parallel Filters	Error Correction	2015
27	An MPCN-Based BCH Codec Architecture With Arbitrary Error Correcting Capability	Error Correction	2015
28	Non-Binary Orthogonal Latin Square Codes for a Multilevel Phase Charge Memory (PCM)	Error Correction	2015
29	A Novel Area-Efficient VLSI Architecture for Recursion Computation in LTE Turbo Decoders	Error Correction	2015
30	Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks	Error Correction	2015
31	Further Desensitized FIR Half band Filters	Matlab + VLSI	2015
32	A Generalized Algorithm and Reconfigurable Architecture for Efficient and Scalable Orthogonal Approximation of DCT	Matlab + VLSI	2015

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33	Novel Design Algorithm for Low Complexity Programmable FIR Filters Based on Extended Double Base Number System	Matlab + VLSI	2015
34	Fully Reused VLSI Architecture of FM0/Manchester Encoding Using SOLS Technique for DSRC Applications	Matlab + VLSI	2015
35	Reliable Radix-4 Complex Division for Fault-Sensitive Applications	Matlab + VLSI	2015
36	Reliable and Error Detection Architectures of Pomaranch for False-Alarm-Sensitive Cryptographic Applications	Cryptography	2015
37	Trade-Offs for Threshold Implementations Illustrated on AES	Cryptography	2015

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38	A 5.8-GHz Wideband TSPC Divide-by-16/17 Dual Modulus Prescaler		2015
39	An efficient constant multiplier architecture based on vertical-horizontal binary common sub-expression elimination algorithm for reconfigurable FIR filter synthesis		2015
40	Low-Power Programmable PRPG With Test Compression Capabilities		2015
41	Efficient Coding Schemes for Fault-Tolerant Parallel Filters		2015
42	A Novel Area-Efficient VLSI Architecture for Recursion Computation in LTE Turbo Decoders		2015
43	An Efficient VLSI Architecture of a Reconfigurable Pulse-Shaping FIR Interpolation Filter for Multistandard DUC		2015
44	Reverse Converter Design via Parallel-Prefix Adders: Novel Components, Methodology, and Implementations		2015
45	Input Vector Monitoring Concurrent BIST Architecture Using SRAM Cells		2014

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