Abstract—Three-level PWM DC-DC converters convert high DC voltage (> 500V) generally at the output of a three phase AC-DC PWM rectifier to an isolated DC output voltage which can be used to power data center loads. Strict efficiency requirements at loads from 20% to 50% of full load of AC-DC converters for telecom applications have been introduced by Energy Star enforcing industries to improve efficiency of the DC-DC converter in an AC-DC converter powering data-center loads at those loads. High efficiency requirements at low and mid loads in high switching frequency PWM DC-DC three level converters implemented with MOSFETs can be achieved by reducing switching losses through optimized load adaptive ZVS for the entire load range. In this paper a simple yet novel load adaptive ZVS auxiliary circuit for three-level converter is proposed for so that the resulting three phase AC-DC converter can meet Energy Star Platinum Efficiency standard. The operation of the proposed DC-DC converter is described, analyzed and validated by experimental results from an industrial prototype of a three phase ac-dc converter comprising of a front end three phase boost PWM rectifier followed by the proposed converter.

Index Terms— DC/DC Converter, Three Level DC-DC Converter, Zero Voltage Switching (ZVS), Coupled Inductor.

I. INTRODUCTION

Three-level DC-DC converters are used for DC-DC conversion with galvanic isolation when the input voltage is typically higher than 500V DC [1]-[22]. Fig.1 shows a three level DC-DC converter. The key advantage of this topology compared to the conventional DC-DC full-bridge converter in high voltage applications is that the input DC voltage is split equally so that the peak voltage stress of the semiconductor devices and the DC bus capacitors is reduced to half of the input DC voltage. This facilitates the use of lower voltage rated semiconductor devices with optimized on-state resistance and smaller parasitic components especially the drain source capacitance of MOSFETs as compared to higher voltage rated devices.

One of the major industrial applications of three level PWM DC-DC isolated converters is in powering network servers in datacenters and telecom devices from three phase utility mains as shown in Fig. 2(a). In such AC-DC converters intermediate DC bus at the output of the front end PWM three phase rectifier can be higher than 500V [11] so that three level DC-DC PWM converter is an ideal converter for accomplishing DC-DC conversion [1]-[23]. Although there exists quite a few three phase AC to DC rectifiers with input power factor correction (PFC) [11], the PWM three phase boost type rectifier shown in Fig. 2 (a) is one of the simplest and cheapest three phase active rectifier which is often used in industrial converters for three phase AC to DC power conversion with input PFC.

In order to reduce overall energy consumption by data centers and telecom loads, U.S. Environmental Protection Agency (EPA), Energy Star and Climate Savers Computing initiative documents, [27]-[30] have set up strict efficiency requirements for converters used in telecom and IT systems and other plug loads powered by the utility mains. According to such regulatory agencies AC-DC converters for plug load applications should have high efficiency values at loads ranging from 20% to 50% of full load to fulfil the strict requirements of Energy Star “Platinum Efficiency Standards”. The corresponding efficiency curve of an AC-DC converter meeting Platinum Efficiency standard is shown in Fig.2 (b). It should also be noted that presently light-load and mid-load efficiencies of such AC-DC converters are of utmost importance compared to the full load efficiency since such
converters always operate in parallel with similar converters along with load cycling so that during their operating cycle these converters mostly operate from 20% to 60% of full load. It is this typical load profile of most frequent operation of the converter that has enforced agency standards like Energy Star to develop such strict efficiency requirements at low and mid loads of a converter. Referring to [29], it can be found that most commercial power supply companies manufacturing power supplies for data center and IT systems prefer to have their power supplies certified by 80PLUS.org in terms of efficiency standards. Herein lays the commercial importance of developing industrial power supplies having efficiencies conforming to standards set by Energy Star. 

It is quite difficult to increase efficiency of front end PWM three phase rectifier [11] without significantly increasing its complexity, so optimizing efficiency of the following DC-DC converter is the best possible way to achieve such efficiency standards introduced by regulatory agencies. This requires the DC-DC converter of an AC-DC converter to have a pretty much flat efficiency graph from 15% of full load to full load with efficiencies typically greater than 95% and that the efficiencies for loads ranging between 20% to 50% of full load should be maximized. This requirement demands optimized load adaptive soft switching in DC-DC isolated three converters [5] or using isolated three level DC-DC resonant converters [19]-[22].

It is essential for the semiconductor switching devices like MOSFETs to operate with zero-voltage switching (ZVS) not only for increasing efficiency but also for reliable operation of the converter from no-load to full load at high switching frequencies (>150kHz). Full range soft switching from no-load to full load is also important for reducing overall EMI of the converter leading to size and weight reduction of the EMI filter components which constitute to the converter weight and volume.

Three level DC-DC converters can be classified into following categories according to the soft switching techniques that they use:

A) **ZCS and ZCZVS PWM three level DC-DC converter:**

ZCS and ZCZVS three level PWM converters have been proposed in [12]-[19]. Zero current switching can reduce switching losses in IGBTs but not in MOSFETs. Hence such converters are either implemented with only IGBTs or combination of IGBTs and MOSFETs and operate at frequencies less than 100 kHz leading to very low power density. Also these converters generally require additional complex auxiliary circuits for realizing soft switching, but soft switching at no load or low loads are not guaranteed.

B) **Resonant three level DC-DC converter:**

In isolated DC-DC converters, achieving ZVS for the entire load range ZVS is relatively easier in resonant converters topologies especially in LLC resonant converters [19]-[22]. One of the key drawbacks of such resonant converters is the complicated control [19]-[22] and their performance is sensitive to variations of resonant tank parameters which are encountered in mass scale manufactured units. Herein lays the importance of PWM DC-DC isolated converters like the well-known PWM DC-DC isolated converters [1]-[18]. Such PWM converters are more robust in terms of controller response and their performance is more immune to parametric variation which arises during mass scale production as compared to LLC and other resonant converters.

C) **Conventional PWM three level DC-DC converter with natural ZVS:**

In PWM DC-DC isolated converters, natural ZVS is mainly achieved by using the energy stored in the transformer leakage inductance of the transformer [1]-[22]; typically, ZVS can be naturally achieved above 60% peak load. The natural ZVS range of a PWM DC-DC three-level converter can be extended by increasing leakage inductance, but doing so causes several problems in the converter operation which are listed below:

a) Loss of effective duty ratio due to the extended dead-time and output diodes’ commutation periods during switching transitions especially during heavy load operation as depicted in ideal waveforms of the converter operation [1]-[18], [23]-[26]. This imposes severe restrictions on the overall load range of the converter [1]-[15], [23]-[26].

b) Increase of leakage inductance creates additional voltage spikes across output rectifier devices [1]-[18], [23]-[26]. This forces the use of lossy snubbers across those devices and also higher voltage rated devices with higher conduction losses will be required to implement the output rectifiers.

c) Increase circulating current in the transformer primary side which increases conduction losses in the primary side devices [23]-[26] of PWM isolated converters and offsets the efficiency gain achieved by soft switching.
Due to the above mentioned issues, it can be concluded that although increasing the leakage inductance can increase the natural soft switching range of the converter but it imposes additional losses and limitations which more than offset the gain in efficiency from soft switching of primary side devices. So external/auxiliary means of creating ZVS in primary side devices without increasing the transformer leakage inductance [1]-[5], [23]-[26] is preferred.

D) ZVS PWM DC-DC Three Level Converters with entire load range ZVS capability:

Several methods of extending the ZVS range in PWM three-level DC-DC converters to less than 60% load have been proposed in the literature in recent past, but most of them fail to achieve ZVS at no load condition. Some of the methods which can achieve ZVS at no load fail to realize load adaptive ZVS over the full load range in the sense that the PWM converters can have natural ZVS at higher loads and do not require additional assistance for doing so. Some of these methods are as follows:

• A Full range soft switching three level converters were proposed in [1]-[3] based on similar auxiliary circuits with inductors connected to the middle nodes of the three level converters to the flying capacitors and DC bus splitting capacitors. The ramp current in the inductors is able to create ZVS for full range. The key drawback is that the ramp current remains constant throughout the load range which is unwanted since at higher loads ZVS can be attained by using energy in the leakage inductor. This causes drop in efficiency at higher loads due to additional conduction losses generated by the circulating currents in the auxiliary circuit. Thus these converters fail to have load adaptive ZVS. Also the excessive amount of inductive current arising at high loads from the constant current peaks of the external inductors can cause very fast discharging of the MOSFET capacitor and subsequent reverse polarity charging if the body diode of the MOSFET is not fast enough, which can lead to failure of the device. Considering, that MOSFET body diode is a slow device in terms of turn off characteristics [23]-[26], [31], constant ramp current ZVS methods may not be suitable for very wide load range operation (typically for load range greater than 0 to 1 kW).

• A passive load adaptive ZVS approach was proposed in [5]. In this topology the circulating current available in the auxiliary circuit was made inversely proportional to the load, which is desired for optimal converter performance. The key problem of the load adaptive ZVS technique reported in [5] is that the auxiliary circuit is placed in series with the main transformer so that the auxiliary winding and the auxiliary capacitors that split the DC bus has to carry the same current as the primary current in the transformer. This results in bulkier components for the auxiliary circuit and also increases the conduction losses due to their parasitic resistances. Moreover, the transformer primary input voltage is reduced to \( V_{DC}/2 \) instead of \( V_{DC}/4 \) in a regular three level converter [1]-[22], causing higher currents and significantly higher conduction losses in the primary bridge devices and passive components for a given load as compared to a basic three level DC-DC converter in [1]-[22].

• Magnetizing currents of transformers can be utilized for ZVS of the three level devices if the converter is implemented with two loosely coupled transformers connected in series [5]. Although this topology has extended ZVS range at low loads but it suffers from some key drawbacks including loss of duty ratio of the converter during charging of the magnetizing inductor and also increased circulating current at mid and high loads due to high amount of magnetizing current. This results in severe restrictions of load range of the converter and efficiency loss at mid and high loads.

• Recently secondary side active control was introduced in PWM three level DC-DC converters to shape the primary current in order to extend the ZVS range of the converter [4]. This method could achieve higher efficiency at mid loads but no load ZVS was not guaranteed by this technique. The use of secondary side active devices and related control results in increased complexity of the converter. Also presence of secondary side diode makes it less attractive for high current loads where synchronous rectifications are essential.

• Three level DC-DC converter with multiple primaries and interleaved secondary’s have been recently proposed in [6]-[8]. These type of converters utilize the additional magnetizing currents of the magnetically coupled multiple transformers for extending ZVS range of the converter. The important drawbacks of these converters include increased circulating currents at mid and full loads, lack of enough magnetizing current for ZVS at low and no loads, increased complexity of the circuit along with increased semiconductors. These drawbacks make them less attractive for industrial applications where cost and complexity of the converter must be minimized.

• It is essential to have an inherent mechanism in the auxiliary circuit so that the circulating current gets reduced as the load current increases. This can be achieved by increasing switching frequency with load as reported in [24], but doing so requires digital control systems and accurate monitoring of output load and transient conditions. Moreover, the use of two separate auxiliary inductors in [1]-[3] and [23]-[26] somewhat reduces the power density that is gained by operating the converter with high switching frequency.

E) Proposed ZVS PWM DC-DC Three Level Converters with load adaptive ZVS:

In order to overcome the issues associated with load adaptive ZVS in three-level PWM DC-DC converters, a new three-level converter topology is proposed in this paper, as shown in Fig. 3. A simple load adaptive ZVS auxiliary circuit consisting of auxiliary inductors \( L_{a1} \) and \( L_{a2} \), DC bus-splitting capacitors \( C_{b1}, C_{b2} \), and flying capacitors \( C_{b3} \) and \( C_{b4} \) which are also involved in the voltage balancing mechanism along with clamping diodes \( D_{a1} \) and \( D_{a2} \) is shown in Fig.3. A DC blocking capacitor \( C_{blk} \) is necessary to block any DC voltage in the transformer primary winding. The auxiliary windings \( L_{a1} \) and \( L_{a2} \) are magnetically coupled with an effective turns ratio of 1:1 and inductance of \( L_{C} \) are the key components of the auxiliary circuit.
Some of the key objectives of this new auxiliary circuit are as follows:
1) Create an external current source by charging and discharging the coupled inductors which will be utilized for ZVS of the bridge devices from no-load to full load
2) The current in the ramp will reduce automatically with increasing load due to its unique magnetic coupling which is essential for reducing conduction losses from circulating currents and also optimize ZVS of the devices since at higher loads the converter can have natural ZVS
3) Coupled inductor will lead to a smaller size of the auxiliary circuit due to the reduced volts-seconds and fewer components.

Other advantages of this auxiliary circuit will be discussed in the subsequent sections of this paper.

The paper is organized as follows:
1) Section-II describes the modes of operation of the proposed converter. In this section, mathematical equations describing current and voltages in key components of the converter are also derived
2) In Section-III the characteristics of the new converter are analyzed based on the mathematical equations derived in Section-II in the pretext of a specific converter as an example.
3) Section-IV validates the feasibility of the proposed converter through practical implementation. In this section operational waveforms of the proposed converter are shown. To emphasize the importance of the proposed converter for meeting Energy Star Platinum efficiency standards discussed earlier, experimental efficiency results of the proposed converter cascaded with a front end three phase PWM AC-DC rectifier, those of the converter in [2] when cascaded with the same AC-DC three phase converter are presented and compared.
4) Section-V presents a comparative study of proposed converter with the conventional PWM three level DC-DC converter and other extended range three level PWM converters in [2], [5]. This section is useful to a practicing engineer to realize the advantages and disadvantages of different three level PWM DC-DC converters before choosing a certain topology for their application.
5) Section-VI is the conclusion

II. MODES OF OPERATION

The modes of operation of the PWM three-level DC-DC converter with the proposed load adaptive ZVS auxiliary circuit are described in this section. Fig. 4 shows the current flow during each mode while Fig. 5 shows the ideal waveforms of the key components of the converter. The converter is controlled by the well-known phase-shift control method, which means that duty ratio of each switch is 0.5 with some dead time; the gating pulses of switches S2 and S3 are complimentary, while those of S1 and S4 are complimentary with a certain phase shift between the gating pulses of S2 and S3 respectively. It is this phase shift that defines the duty ratio of the transformer primary voltage \( V_{ab} \) and in turn, controls the output voltage.

The clamping diodes \( D_{c1} \) and \( D_{c2} \) are provided to equalize the voltage across the semiconductor devices and to clamp the voltage \( V_{ab} \) to zero whenever necessary. The coupled inductor is modeled as an ideal transformer with two windings \( L_{ab}, L_{ac} \) of turns ratio of 1:1 and a magnetizing inductance \( L_c \). In this context, it is worth mentioning that the current in an auxiliary inductor is considered positive when flowing into its dotted end and the voltage across the inductor is considered positive when the potential of its dotted end is greater than that of its other end. Current in the transformer primary is positive when it flows from node a to node b.

At any time instance, the following relation holds good for the coupled inductor:

\[
i_{L_{ac}} = -\frac{i_{L_1}}{2} \quad \text{and} \quad i_{L_{ab}} = +\frac{i_{L_1}}{2}
\]  

(1)

The steady state voltages \( V_{cb3} \) and \( V_{cb4} \) across the capacitors \( C_{b3} \) and \( C_{b4} \) should be \(+V_{DC}/4\). Due to the symmetrical operation of the converter over each half of the switching cycle, only the operation of the converter during half a switching cycle is discussed in this section.

Mode-1(\( t \neq t_1 \)): This is an energy transfer mode. Switches \( S_1 \) and \( S_2 \) are conducting and energy is transferred from the upper DC bus capacitor \( C_{b1} \). The transformer primary voltage \( V_{ab} \) is equal to \( V_{DC}/2 \). Voltage \( V_{ac} \) across \( L_{ac} \) is \(+V_{DC}/4\) so that the net voltage across the coupled inductor \( L_c \) during this mode is zero so the current in it remains constant. Also during this mode, a net positive voltage of \((V_{DC}/2-V_{N})\) is incident across the combination of leakage inductance \( L_{lk} \) and the reflected output inductor to the primary side so that the current in them starts increasing. The key equation in this mode is:

\[
i_{L_1}(t) = i_{L_1}(t_0) + \frac{V_{DC}}{N^2 L_{o1} + L_{lk}}(t - t_0) \quad \text{for} \quad (t_0 < t < t_1)
\]

(2)
Fig. 4 Equivalent circuits for modes of operation
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This mode ends with the voltage across $S_1$ rising to $V_{DC}/2$.
During modes 1 and 2 current in $L_{a1}$ is negative and current in $L_{a2}$ is positive.

**Mode-3($t_3$-$t_4$):** This is a freewheeling mode with no energy being transferred to the output through the transformer, whose primary remains shorted in this mode. The clamping diode $D_{c1}$ starts to conduct and clamps the voltage of $S_1$ at $V_{DC}/2$ while the voltage across $S_2$ is zero. During this mode, there is a change in the voltage waveform of the coupled inductor $L_{a1}$ so that a new positive voltage of $+V_{DC}/4$ is incident across $L_{a1}$ and a new negative voltage of $-V_{DC}/4$ reflected from $L_{a1}$ is incident across $L_{a2}$. In this mode, current in $L_{a1}$ begins to ramp up while that in $L_{a2}$ starts to ramp down; the output current flows through diode $D_{c1}$. At the end of this mode, the inductor currents reverse their polarities at time $t_3$. The slopes of the current in the coupled inductors are given by $V_{DC}/4L_{a1}$ in $L_{a1}$ and $-V_{DC}/4L_{a2}$ in $L_{a2}$. Also during this mode, a net negative voltage of $-V_{a}N$ is incident across the combination of leakage inductance and the reflected output inductor to the primary side so that the current in them starts reducing. Sometimes during this mode, switch $S_1$ can be turned on with ZVS.

**Mode-4($t_4$-$t_5$):** At $t_3$, the currents in the coupled inductor reverse their polarities and continue to slew at the same rate as given in Mode-3. The current in switch $S_2$ also reverses in this mode and flows through the bulk device. The transformer primary voltage $V_{ab}$ still remains clamped to zero. Switch $S_2$ is turned off at the end of this mode.

It should be noted that the combined duration of Mode-3 and Mode-4 signify the zero state of the transformer primary voltage over half a switching cycle.

The key equation for the transformer primary current during modes 3 and 4 is given by:

$$\frac{d}{dt}i_{ik}(t-t_2) = -\frac{NV_{o}}{(L_{a0}+N^2L_{o})} \text{ for } (t_2 < t < t_4) \quad (5)$$

The duration of the combined mode 3 and 4 signify the zero state of the transformer primary voltage over half a switching cycle and is given by:

$$(t_4 - t_2) \approx (1-D)\frac{T_{sw}}{2} \quad (6)$$

While the currents in the two auxiliary windings are:

$$i_{aux1} = i_{aux1}(t_3) + \frac{V_{DC}(t-t_4)}{16L_{aux1}} \text{ for } (t_2 < t < t_4) \quad (7)$$

$$i_{aux2} = i_{aux2}(t_3) + \frac{-V_{DC}(t-t_4)}{16L_{aux2}} \text{ for } (t_2 < t < t_4) \quad (8)$$

So the net change in current in the auxiliary windings during the combined modes 3 and 4 is:

$$\Delta i_{aux} = \frac{V_{DC}(1-D)T_{sw}}{16L_{aux2}} \quad (9)$$

Since no DC can flow through each of the auxiliary windings, the magnitude of the peak ramp current in each winding during mode-1 and Mode-2 is:
The above equations are derived based on the assumption that the auxiliary inductors are much larger in value than the leakage inductor so that current in auxiliary inductor remains constant at \( i_{aux}(t_4) \) during this mode.

The equations describing the switch voltages during this mode are:

\[
v_{\text{Sw}2}(t_4) = \frac{V_{\text{DC}}}{2} \cos \omega_t (t-t_4)
\]
\[
v_{\text{Sw}2}(t_4) = \frac{V_{\text{DC}}}{2} \sin \omega_t (t-t_4) - \frac{i_{aux}(t_4)}{2C_{\text{ds}}} (t-t_4)
\]
\[
v_{\text{Sw}3}(t_4) = \frac{V_{\text{DC}}}{2} \cos \omega_t (t-t_4)
\]
\[
v_{\text{Sw}3}(t_4) = \frac{V_{\text{DC}}}{2} \sin \omega_t (t-t_4) - \frac{i_{aux}(t_4)}{2C_{\text{ds}}} (t-t_4)
\]
\[
i_{l_k}(t-t_4) = \frac{N V_o}{(L_{o1} + N^2 L_{o2}) \omega_t} \sin \omega_t (t-t_4)
\]
\[
i_{l_k}(t-t_4) = \frac{N V_o}{(L_{o1} + N^2 L_{o2}) \omega_t} \cos \omega_t (t-t_4)
\]

Where \( \omega_t = \frac{1}{\sqrt{2L_n C_{\text{DS}}}} \) (17)

And \( i_{l_k}(t_4) = \frac{I_o}{N} \left( \frac{V_o}{(L_{o1} + N^2 L_{o2})} \frac{1-(D) |T_{\text{sw}}|}{2} \right) \) (18)

At the end of this mode, clamping diode \( D_3 \) stops conducting.

Mode-6 (\( t_6-t_7 \)): This mode is similar to mode-5 except that the body diode of \( S_1 \) starts conducting so that \( S_3 \) can be turned on with ZVS. This mode ends with the transformer primary reducing to zero and undergoing phase reversal at time \( t_6 \). From this mode onwards till the turn-off of \( S_3 \), the transformer primary voltage remains clamped to \(-V_o/2\).

During mode-6 current in \( S_4 \) can flow either through the bulk device or through its body diode depending on the magnitude of the currents in the transformer primary and the currents in the coupled inductor.

Mode-7 (\( t_7-t_8 \)): At \( t_7 \), the transformer primary current starts reversing its phase and increases in a reverse direction until the magnitude of the current in the leakage inductor equals the current in the output inductor reflected at the transformer primary side at time \( t_8 \) during steady state operation of the converter. At time \( t_7 \) another energy transfer mode begins and output diode \( D_{o2} \) conducts the transformer secondary current and \( S_3 \) and \( S_4 \) are conducting the transformer primary current.

The equation describing the current in the leakage inductor during this mode is given by:

\[
i_{l_k}(t-t_8) = \frac{V_{\text{DC}}}{2L_{n k}} (t-t_8) \text{ for } (t_6 < t < t_7)
\]

The negative sign in equation (19) signifies the fact that the transformer leakage inductor current is now flowing in the reverse direction from node b to node a.

It should be noted that duration of this mode signifies lost duty ratio of the converter. So it is imperative to reduce the duration of this mode and the most effective way to do so is to reduce the leakage inductor.

Between modes-5 to 7 the output inductor current continues to freewheel through \( D_3 \) and \( D_{o2} \) with a negative voltage of \(-V_o\), so that the current in the output inductor during this duration \( t_4 \) to \( t_7 \) is given by:

\[
i_{l_k}(t-t_4) = \frac{V_o}{L_{n k}} (t-t_4) \text{ for } (t_4 < t < t_7)
\]

The following can be concluded from the above discussion on the modes of operation:

- It is this current given by equation (9), available from the coupled inductor which is responsible for assisting ZVS of the bridge devices during Mode-2 and Mode-5. The current given by equation 10 is extremely significant in the sense that it signifies the peak ramp current magnitude in the coupled inductor and it is now a function of the duty ratio of the converter. The growth of ramp current in the auxiliary inductors depends on the duration of the non-energy transfer modes or the freewheeling modes i.e. Modes 3 to 5 which is approximately \((1-D)|T_{\text{sw}}|/2\). The ramp current magnitude will be greater at lower loads when Modes 3 to 5 are longer because of the smaller duty
ratio of the converter, while the same ramp will have less opportunity to slew at higher loads when the duration of Modes 3 to 5 are shorter. The assistance from the auxiliary circuit is most needed in terms of the ramp current during switching intervals at low loads when there is not enough energy in the leakage inductance to discharge switch capacitors, while the same assistance from the auxiliary circuit needs to be minimized as load increases since the energy in the leakage inductance increases as well leading to natural ZVS at higher loads. This feature is achieved by the proposed coupled inductor auxiliary circuit, which is simple, unique and novel. Quantitative analysis of the load adaptive characteristic of the proposed auxiliary circuit will be shown in Section III of this paper.

- ZVS at no load is easily achieved since the ramp current magnitude is at its maximum at no load and can provide the sufficient amount of inductive current for discharging switch capacitances.
- The component count of the converter is reduced and better component packaging can be achieved by having a coupled inductor auxiliary circuit instead of separate auxiliary inductors wound on separate cores.

III. ANALYSIS AND DESIGN

In this section, some of the key aspects of the converter operation are analyzed based on the modes of operation and the related equations derived in section-II. Characteristics of the converter in terms of some important parameters are also derived. The analysis is based on an example specification as follows:

a) Input DC voltage: \( V_{DC} = 800\text{V} \)

b) Switching Frequency: \( f_{sw} = 200\text{kHz} \)

c) Output Voltage: \( V_o = 12\text{V} \)

d) Output Power \( P_o \) varies from 0 to 2.5kW.

e) Transformer turns ratio: 24:1

f) Output Inductor: 1 \( \mu \text{H} \)

A. ZVS Condition for Switch Pair \( S_1, S_2 \):

The ZVS condition for the outer switch pair \( S_1, S_2 \) is different from that of the inner switch pair \( S_3, S_4 \) due to the involvement of the output inductor during the switching instances of \( S_1 \) and \( S_2 \) as depicted in Mode 2 of operation. The condition for soft switching of these switches at loaded condition of the converter is given by:

\[
\frac{V_{dc}}{2} = \frac{I_{nk}(t_f) + I_{aux1}(t_f)}{C_{DS}} T_D \tag{21}
\]

Where

\[
i_{aux1}(t_f) = i_{auxpk} = \frac{V_{dc}(1 - D) T_{sw}}{32L_{aux2}} \tag{22}
\]

And

\[
i_{nk}(t_f) = I_o + \frac{V_{DC} - V_o}{L_{nk} + N^2 I_o} T_{sw} \tag{23}
\]

In case of no load when \( i_{nk}(t_f) \) is negligibly small then the ZVS condition will be:

\[
\frac{V_{dc}}{2} = \frac{i_{aux1}(t_f)}{C_{DS}} T_D
\]

In Figs.6 (a) and (b), the required deadtime for ZVS of \( S_1 \) and \( S_4 \) at no load and at different load currents for a leakage inductor of 1.2\( \mu \)H are plotted. In this case the value of the leakage inductance is kept so low to reduce loss of duty cycle described in the modes of operation and also to reduce the peak voltage stress across secondary side rectifier [5, 23]-[27]. It should be noted that the switch capacitance is highly non-linear and is a function of the MOSFET drain to source voltage, the non-linearity is especially prominent at voltages of 200V and less, so it has to be accurately evaluated from the characteristic log linear graph of \( C_{oss} vs V_{DS} \) in the datasheet [31] of the MOSFET. Fig. 6(a) shows the amount of dead time necessary to discharge the switch capacitance at no load for different amount of auxiliary circuit peak current. Fig. 6(b) shows the requirements of auxiliary circuit current for different amounts of dead time in loaded condition. As the load current increases so does the energy stored in the combination of leakage inductor and the reflected output inductor. Due to the increased amount of energy in this combination of inductors, faster discharging of the switch capacitances of \( S_1 \) or \( S_2 \) occurs and also lesser amounts of peak auxiliary circuit currents are required at higher loads; these facts are quantitatively depicted in Fig. 6. Herein lays the importance of reducing the auxiliary ramp current in a load adaptive fashion with increasing load in a PWM three-level DC-DC converter.

In this case an important design trade-off needs to be made and that is the maximum dead-time which can be allowed and the amount of the assistance from the auxiliary inductor \( L_{aux} \) at no load or at lower loads. It is critical to reduce conduction losses along with reducing switching losses at low loads so as to minimize overall losses in the converter which is important to meet the high efficiencies at such low loads. Again, on the other hand too low assistance from auxiliary circuit may result in longer dead times or failure of proper ZVS turn-on which is not desirable.

From the characteristics graphs a dead time of around 270\( \text{ns} \) at no load can be chosen along with a no load ramp current peak of 1.8 Amps can be chosen. It should be noted that the dead time which is implemented on the gating pulses of \( S_1, S_4 \) is made load adaptive by use of the PWM controller UCC2895 from TI [33] and a variation of this dead time is 130\( \text{ns} \) to 270\( \text{ns} \) from full load to no load is favored since it conforms with the speed of the typical analog circuitry involved with the gating circuitry for these devices. In this case the designer should be careful to choose the range of this dead time so that it is not too high which will reduce the effective duty ratio of the converter or too low compared to the delays in the involved analog gate drive circuitry.

At this point the designer should also confirm if this amount of ramp current is also suitable for ZVS of the inner devices too, which is discussed in the next sub-section.

B. ZVS Condition for Switch Pair \( S_3, S_4 \) during turn on:
The zero voltage switching of the switches \( S_2 \) and \( S_3 \) are more critical than those of \( S_1 \) and \( S_4 \), since during the switching transitions of these switches there is no involvement of the larger output filter inductor reflected to the primary side as described by Mode-5. The equivalent circuit involved during this mode without and with the auxiliary circuit is shown in Figs. 7(a) and (b), assuming that the auxiliary inductor is much larger than the leakage inductor so that it maintains a constant current during the switching instance of the devices \( S_2, S_3 \) signified by Mode-4 of operation when \( S_2 \) is turned-off.

Without the assistance of auxiliary inductor current, the output capacitances of switches \( S_2 \) and \( S_3 \) charge and discharge to and from \( D_{s1}/2 \) while resonating with the leakage inductor; so enough energy must be stored in the leakage inductor at time \( t_4 \) so in order to ensure natural ZVS of these switches. This condition is approximately given by [27]:

\[
\frac{1}{2} L_{lk} \left[ i_{lk}(t_4) \right]^2 \geq \frac{4}{3} C_{oss} \left( V_{DS} \right) \frac{V_{DC}^2}{4}
\]

(25)

The most notable aspect of this equation is that at no load or very low loads typically less than 20% of full load, when transformer primary current is very small, ZVS switching of devices \( S_2 \) and \( S_3 \) is not possible and herein lies one of key drawbacks of PWM three level or two level converters [1]-[27]. Referring to equivalent circuits in Fig.7 it can be realized that the ramp peak current is extremely essential for ZVS of these devices at low loads. Also note that similar situation occurs for outer devices \( S_1 \) and \( S_2 \), turn on and turn-off except that reflected output inductor is involved in series with the leakage inductor.

Figs. 8(a) and (b) show the amount of leakage inductor required for ZVS turn on of these devices and the required dead time for achieving ZVS naturally through stored energy in the leakage inductor. From both of these figures it can be inferred that for extending ZVS range of devices \( S_2 \) and \( S_3 \) not only a very large leakage inductance will be necessary but also a large amount of dead time will be required, which will cause a huge amount of loss of duty ratio of the transformer primary voltage. Thus without assistance of the auxiliary circuit ZVS of these switches cannot be realized below certain output loads [1]-[18], [23]-[26]. Moreover it should also be noted leakage inductor in the transformer has to be kept small for two fundamental reasons, one of them being minimizing the loss of duty ratio of the converter signified by the mode-6 of operation and also to reduce the voltage stress across output rectifier devices [1]-[18], [23]-[26]. Excessive voltage spike across the secondary side rectifier should be avoided so as to enable use of lower voltage rated more efficient devices for synchronous rectification in case of high current applications like powering network servers.

An important phenomenon that occurs during the switching transition of this mode is the reduction of the leakage inductor current to zero and its consequent phase reversal in the following mode-6 as described in Section-II mode-5 and mode-6. Mostly at low loads there is not enough energy stored in the leakage inductor to completely discharge the MOSFET output capacitance during mode-5 of operation. In such case the voltage across the MOSFET output capacitance \( C_{DS} \) discharges by resonance with the leakage inductor to a finite valley voltage \( V_{v,less} \) than the off-state voltage across the device, following which \( C_{DS} \) will again charge up from this voltage \( V_s \) due to phase reversal of current in the leakage inductor till the switch is turned on in Mode-6 as shown in Fig. 9. To overcome this key problem and achieve ZVS of switches \( S_2 \) and \( S_3 \), the peak value of the ramp current in the auxiliary inductors should be enough to overcome the effect of the phase reversal of the leakage inductor and discharge the switch capacitors. The voltage across the device undergoing partial ZVS during such a transition in the absence of any auxiliary circuit will be given by:

\[
v_{s}\left(t-t_4\right) = \frac{V_{DC}}{2} \cos \omega_c\left(t-t_4\right) - \frac{i_{lk}(t-t_4)}{2 C_{DS} \omega_c} \sin \omega_c\left(t-t_4\right)
\]

(26)
Figs. 10 shows the characteristic graphs of the proposed converter for the soft switching of the devices $S_2$ and $S_3$ if no auxiliary circuit is provided. In Fig. 10(a), the time in which the current in the leakage inductor reduces to zero and reverses in phase during the modes-5 and 6 as a function of the current in the transformer primary at the end of Mode-4, is plotted. This graph is important in the sense that it gives a measure of the actual time window available for soft switching of the devices $S_2$ and $S_3$, at low loads this phase reversal time is quite short (140ns) and herein lies the issue of the switch capacitor charging up after reaching the valley voltage; the actual voltage from which the switch will be turned on in the absence of the auxiliary circuit, as a function of leakage inductor for different dead times is provided in Fig. 10(b).

Fig. 11 shows the magnitude of the auxiliary inductor ramp current necessary for soft switching of $S_2$ or $S_3$ for the device in [31] as a function of current in the leakage inductance at the end of Mode-4 and for different dead times. This curve is essential to design the auxiliary inductor. In this case an important trade-off must be made. This trade-off is that the auxiliary inductor current peak value should be enough to ensure ZVS turn on of $S_2$ and $S_3$ for all loads and reduce the loss of effective duty ratio the transformer primary voltage; again on the other hand increased amount of auxiliary inductor peak current will lead to conduction losses in the devices especially at low loads and also copper losses in the auxiliary inductors. Another key factor of choosing the dead time for the devices is the consideration of the delays involved in the analog devices involved in the gate driver circuitry as mentioned in the previous sub-section. From Fig. 11, the value of peak auxiliary inductor current is chosen to be 1.8Amps specified by the characteristic curve drawn for a dead time of 270ns. From the same graph in Fig. 11 it can be seen that as load increases for a fixed dead time the amount of peak auxiliary inductor current required also decreases since the leakage inductor energy at the end of Mode-4 increases with load and aids ZVS turn-on naturally.

In this context, one should also keep into consideration that the use of auxiliary inductance for ZVS of bridge devices can pave the way for reducing both the leakage inductance and the dead time since no longer is soft switching dependent on the energy stored in the leakage inductor. As mentioned before reduction of leakage inductance has two fold benefits, it leads to reduction of output rectifier voltage spike [1]-[18], [23]-[26] and also reduction of duration of modes-5, 6 and 7 so that...
the effective duty ratio of the converter can be maximized.

C. ZVS turn-off of the bridge devices:

Another significant phenomenon that is shown in Fig. 7 is the turn off mechanism of the MOSFETs. It can be realized from Fig. 7, that presence of the auxiliary circuit current has the effect of speeding up the charging process of the output capacitance during turn-off of the MOSFET due to additional inductive current from the auxiliary circuit. Especially at high loads, the currents in the transformer leakage inductor and the non-coupled auxiliary circuit can be large enough during turn-off of devices S1 or S4, which can result in abrupt charging of their output capacitances. If this charging process is faster than the finite fall time of the device [30] then significant turn-off losses can also occur. So for proper ZVS turn-off of the MOSFET device, it must be ensured that the turn-off process is longer than the fall time of the device.

D. Load adaptive behavior of the auxiliary coupled inductors:

In this sub-section the load adaptive behavior of the proposed auxiliary circuit is discussed. Before going into further details the operation of the practical DC-DC PWM three level converter will be discussed first. In this context it should be noted that in data center applications, the output voltage is low but the output DC current is high (of the orders of 100Amps or more depending on the maximum output power). In such cases if the output filter inductor is made very large to satisfy continuous operation at lower loads (<15% full load), then either its physical size or its copper losses will be very high. Typically in such high current output converters, the output inductor is kept low around 1µH [24] so that the inductor can be implemented with just one turn on a planar core as will be discussed in next section. Owing to these fundamental and practical reasons an industrial DC-DC converter will have variation in its operating duty ratio as the load varies. The duty ratio of the DC-DC three level converter will increase with increasing output load because of the loss of effective duty cycle due to the existence of mode-6 of operation [5], [24] to overcome the losses in the converter and also whether the output inductor current will be in continuous or discontinuous mode [33]. Mathematical details for plotting Fig. 12 (a) can be found in [33] and subsequently solving the following steady state voltage conversion ration of the PWM three level DC DC converter as follows:

\[
V_o = \frac{2}{N} \left[ V_{DC} - 2 I_{pri, rms} R_{DS,on, pri} \right] - I_{o, rms} (R_{DS,on, syncrec} + R_{ESR, L_o} + R_{Trans, sec}) N D
\]

for continuous output current

\[
V_o = \frac{2}{1 + \sqrt{1 + \frac{4K}{D^2}}}
\]

for Discontinuous output current,

Where \( K = \frac{2L_o N^2}{R_o T_{sw}} \), \( I_{pri, rms} = \frac{1}{N} \sqrt{\left( \frac{V_o}{R_o} \right)^2 + \frac{\Delta I_o^2}{12}} \) \( L_o \) is the output inductor, \( I_{o, rms} \) is the rms current in each output synchronous rectifier, \( I_{pri, rms} \) is the primary side rms current,
N:1 is the transformer turns ratio, \( I_{\text{pri},\text{rms}} \) is the rms current in transformer primary voltage, \( R_{\text{DS,on,pri}} \) is primary MOSFET on state resistance at operating temperature, \( R_{\text{DS,on,syncrec}} \) is secondary synchronous rectifier MOSFET on state resistance at operating temperature, \( R_{\text{Trans, pri}} \) is the AC resistance of transformer primary winding, \( R_{\text{Trans, sec}} \) is the secondary winding AC resistance, \( R_{\text{ESR,Lo}} \) is the series resistance of output inductor and \( \Delta I_\mu \) is the peak to peak output ripple current.

The peak ramp current in the auxiliary inductor is given by equation 10 in Section II. The auxiliary peak current for different duty ratios load currents is plotted in Fig. 12 (b) for \( V_{\text{DC}}=800\text{V}, L_{\text{aux}}=140\mu\text{H}, f_{\text{sw}}=200\text{kHz} \). Fig. 12 (c) shows the variation of the auxiliary ramp current as a function of the output load current. In this figure a plot of the ramp current due to two non-coupled separate auxiliary inductor as a function of load current is also shown.

It can be concluded from Fig. 12, that as the duty ratio of the converter increases with increase in load current, the peak current in the auxiliary inductor available for ZVS of the bridge devices gets reduced which in turn reduces the circulating current in the converter and also optimizes the net amount of inductive current necessary for ZVS with as a function of load.

E. Design of auxiliary inductor:

The coupled inductor required is AC in the sense that the ramp current is bipolar. So in this case maximum volts-second during each half switching cycle is the key factor which should be considered for designing the inductor. The volts second across this coupled inductor can be derived from the modes-4 and 5 of operation of the proposed converter when finite voltage exists across the coupled inductor as shown in Fig.5. From Fig.5, the key equation dictating the design of the auxiliary inductor is given by:

\[
N_{\text{aux}} \geq \frac{V_{\text{DC}}}{16} \left(1 - d\right) \frac{(1 - d)}{10^8}
\]

Where \( \Delta B_{\text{max}} \) (Gauss) is the peak flux density of the core material being used, \( N_{\text{aux}} \) is the number of turns of each auxiliary inductor, \( A_e \left(\text{cm}^2\right) \) is the cross sectional area of the core being used. A ferrite core is used to implement the coupled inductor and the inductance is adjusted by properly gapping the core.

The gap needed for the inductance should be calculated precisely considering the fringing flux effect around the gap, placement of the winding and the core shape. In this case the well-known McLymann’s formula [31] for the fringing flux effect is used as follows:

\[
F = [1 + \frac{\ell_g}{\sqrt{A_e}} \ln \left(\frac{2G}{\ell_g}\right)]
\]

So that the inductance in the gapped core is given by:

\[
L_{\text{aux}} = \frac{0.4\pi N^2 A_e F}{\ell_g}
\]

The value of this inductance should be same as the value of the coupled inductor necessary for the largest value of the ramp current which occurs at no-load operation of the converter and it is given by equation (10) as follows:

\[
I_{\text{aux}} = \frac{V_{\text{DC}}(1 - D_{\text{min}})T_{\text{sw}}}{32I_{\text{aux, pk}}}
\]

It is well known from fundamentals of magnetics design that volts-seconds of ac inductor are the key design parameter which determines the physical size of the inductor core [32]. In this context it is quite interesting to compare the inductor size for the proposed auxiliary coupled inductor and the auxiliary inductor proposed in [1]-[3], [23]-[26]. The design criteria for the inductor in [1]-[3] can be written as:

\[
N_{\text{aux}} \geq \frac{V_{\text{DC}}}{16} \frac{1}{f_{\text{sw}} A_e \Delta B_{\text{max}}}
\]

Comparing equations (30) and (31) it can be concluded that the volts seconds across the coupled inductor is less by the factor of \( (1 - D_{\text{min}}) \) which implies that the core size for the coupled inductor is smaller than the non-coupled inductor.
IV. EXPERIMENTAL RESULTS

An experimental prototype of the proposed converter and the converter proposed in [2] were implemented with the key specifications as shown in Table I. The implemented circuit is shown in Fig. 13. Table II shows the key components of the DC-DC converter. Three-level switches were implemented with SPW47N60C1D. This is a silicon super junction MOSFET from Infineon with a fast body diode.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Po</td>
<td>Output Power</td>
<td>2.5KW</td>
</tr>
<tr>
<td>Vac</td>
<td>Input Voltage</td>
<td>3 phase220V–420V line to line</td>
</tr>
<tr>
<td>Vdc</td>
<td>Intermediate DC bus</td>
<td>800V DC</td>
</tr>
<tr>
<td>Vo</td>
<td>Output Voltage</td>
<td>12 V DC</td>
</tr>
<tr>
<td>f_o</td>
<td>Three phase PWM boost switching frequency</td>
<td>30KHz</td>
</tr>
<tr>
<td>f_sw</td>
<td>Three level-Bridge Switching Frequency</td>
<td>200 KHz</td>
</tr>
<tr>
<td>I_int(max)</td>
<td>Maximum input current</td>
<td>6 Amps per phase</td>
</tr>
<tr>
<td>P.F.</td>
<td>Power Factor</td>
<td>&gt; 98%</td>
</tr>
</tbody>
</table>

For the high current output, current doubler synchronous rectification was implemented. Output synchronous rectifiers were implemented with three parallel BSC016N06NS in each row. A RC snubber of 1 ohm, 1nF capacitor is implemented across each set of synchronous rectifiers.

The output inductors were implemented on two sets of planar EE-43-3C94 cores with one turn of 5 mm thick copper bar and a gap of 0.3 mm on the center leg. Planar EE-43-3C94 core was used for the transformer. The transformer has turns ratio of 12:1 with current doubler rectifier which is equivalent to 24:1 on a regular rectifier. Leakage inductance measured on the transformer was 1.57μH which reduced voltage spike across output rectifier and the loss of duty cycle of the DC-DC converter.

The auxiliary coupled inductor was implemented on a PTS23/18-3C91 core with 60 turns of 24 AWG litz wire having 42AWG strands. A gap of 0.6mm was provided at the center leg. The value of the coupled inductor was 140μH each. The controller used to control this converter is T1 UCC2895 [33]. It should be noted that non coupled inductors were also implemented with magnitude of the peak current of about 1.8Amps for the sake of comparison.

A standard front-end AC-DC three phase boost PWM rectifier with continuous conduction of input current was further implemented and the three level AC-DC converter were cascaded with this front end active rectifier in order to develop a three phase AC-DC converter suitable for data center application. This is done to validate the overall efficiency of the AC-DC three phase converter with the same front end converter but with different type of ZVS on the three
level DC-DC PWM converter. The AC-DC converter was energized by a three phase utility mains input of 380V line to neutral, the output voltage of the front end rectifier was 800V dc which gives rise to the intermediate DC bus input to the three-level DC-DC converter. The front end PWM AC-DC rectifier had IGBT devices and was operated at 30 kHz switching frequency. Efficiency graphs of the overall ac-dc system will be shown and discussed in this section. In this context it should be noted that three phase PWM boost rectifier is normally chosen for such application because of its low cost and simplicity to implement although there are different types of front-end three phase rectifier topologies are available [11].

Fig. 14 shows the ramp current at full load. It can be seen in Fig.14, that the ramp current remains constant when the transformer primary voltage is non-zero and it slew s only when the transformer primary voltage is zero.

Fig.15(a), and (b) shows the ramp current at 5% of full load and at full load without magnetic coupling of the auxiliary inductor as shown in [1]-[3]. Comparing the two Figs. 14 and 15 it can be concluded that the unique magnetic coupling of the auxiliary windings is the key to make the ramp load adaptive so that the ramp current excursions are maximum at no load and continues to decrease as load is increased while the same phenomenon is absent when non coupled inductors are implemented as suggested in [1]-[3].

Fig. 16 shows the transformer primary voltage and the transformer secondary voltage at full load. It should be noted that the time difference between the rise time of the transformer primary voltage and that of the transformer secondary voltage is 75ns which signifies a loss of duty ratio by only 1.5% as described in mode-7 of the converter; also the peak voltage across the synchronous rectifier is 45Volts, herein lies the practical importance of reducing the leakage inductance of the transformer.

The magnified waveforms of drain source and gate source voltages of S1 at different loads are shown in Fig.17 and Fig18. Fig. 19 shows the ZVS turn on of S1 at no load and Fig.18 shows ZVS turn on of S1 at 80% of full load. The switching transition of S1 shows no overlapping of MOSFET drain to source voltage and gate source voltage during turn-on which clearly confirms ZVS turn on of this device at no load and at high loads too. One more notable aspect in the Figs. 17 and 18 are the variation in the slope of the voltage across the device S1 at different loads, this is due to the fact that at higher loads there is more current in the series combination of leakage inductor and reflected output inductor on the primary side which causes faster slew rate of the voltage across S1 at higher loads.

Fig. 19 shows the turn on of S2 at no load, and Figs. 20, 21 and 22 shows the turn-on of device S2 at no load, 20% of full load, 40% of full load and 60% of full load respectively. In each of these figures, it can be seen that the MOSFET drain to source voltage reduces to zero and then the MOSFET gate source voltage rises, which implies that the MOSFET

<table>
<thead>
<tr>
<th>TABLE II</th>
<th>CONVERTER PARAMETERS</th>
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</thead>
<tbody>
<tr>
<td>Symbol</td>
<td>Parameter</td>
</tr>
<tr>
<td>C_B1, C_B2</td>
<td>Intermediate DC Bus Capacitor</td>
</tr>
<tr>
<td>C_blk</td>
<td>DC Blocking Capacitor</td>
</tr>
<tr>
<td>C_o</td>
<td>Output Capacitor</td>
</tr>
<tr>
<td>L Aux</td>
<td>Auxiliary Inductor</td>
</tr>
<tr>
<td>L_o1, L_o2</td>
<td>Current doubler output Inductors</td>
</tr>
<tr>
<td>N:1</td>
<td>Turns Ratio of Power Transformer (Primary: Secondary)</td>
</tr>
<tr>
<td>L_k</td>
<td>Primary Leakage Inductance</td>
</tr>
<tr>
<td>S1, S2, S3, S4</td>
<td>Power MOSFETs</td>
</tr>
<tr>
<td>D_C1, D_C2</td>
<td>Clamping diodes</td>
</tr>
<tr>
<td>S_r1, S_r2</td>
<td>Output Synchronous rectifier</td>
</tr>
</tbody>
</table>

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undergoes zero voltage turn-on.

There are some notable aspects of the voltages across $S_2$ and $S_3$ in Figs. 19-22 and they are the different slopes of the MOSFET drain to source voltage waveform while the voltage is reducing before turn-on. This is due to the fact that the MOSFET voltage initially decreases predominantly resonating with the leakage inductor till it reaches the kink on its falling edge which signifies the fact that the leakage inductor current reverses in phase at that time instant and subsequently the switch voltage decays with the help of the ramp current so that the lower half of the falling edge slews with a different slope. Thus the magnified waveforms of ZVS turn on of $S_2$ and $S_3$ at different loads validate this important phenomenon described in Section-IV. Fig. 23 shows the turn-on waveform of the device $S_3$ at 70% of full load without any auxiliary circuit. It can be seen that due to the very low value of leakage inductance chosen for the three level converter, complete natural ZVS of devices $S_1$ and $S_3$ cannot occur even at around 70% of full load.

Figs. 24 show the turn-off of device $S_4$ at 50% load. Fig. 24 (a) shows turn-off of the device $S_4$ with coupled inductor while Fig. 24 (b) shows the turn-off of $S_4$ with non-coupled auxiliary inductors. It can be seen that during turn off, the rise of drain to source voltage across the device occurs much slowly in case of proposed approach than the two non-coupled inductor approach proposed previously [1]-[3] due to excessive amount of inductive current arising from the non-coupled auxiliary inductors than the coupled inductor in which the ramp current is load adaptive and decreases with increase of load. Faster turn-off of the device and faster rise of voltage across it during turn-off is due to extra inductive current in the circuit. This leads to turn-off loss of the device due to its finite amount of fall time which in this case is 85ns. This is another important feature of the proposed approach that contributes towards increased efficiency at mid loads.

For measuring efficiency, procedures [35] set up by joint committee of EPRI and Ecova Plug Load Solution responsible for certifying efficiencies of such converters were followed. Efficiency of the proposed DC-DC three level PWM
The proposed converter is over 95% efficient above 20% of full load and exhibits a flat efficiency graph for loads between 20% of full load to full load. This figure also shows the efficiency of the same converter with non-coupled auxiliary inductors [1]-[3].

It can be concluded that the new converter with coupled auxiliary inductor is significantly more efficient than the non-coupled topology for loads above 10% of full load and this can be attributed to the novel yet simple load adaptive auxiliary circuit implemented in the proposed converter which optimizes the soft switching of the device for all over the load range resulting in superior efficiency and reliable operation of the converter for the whole load range from no load to full load.

Fig. 20. ZVS turn on of \( S_3 \) at 20% of full load (C1:5 V/div, C2: 100V/div, t: 250ns/div)

Fig. 21. ZVS of \( S_3 \) at 40% of full load (C1:100V/div, C2:10V/div, t: 200ns/div)

Fig. 22. ZVS of \( S_3 \) at 60% of full load with coupled inductor (C1:100V/div, C2: 10V/div, t: 100ns/div)

Fig. 23 Turn on waveform of \( S_3 \) without any auxiliary circuit at 70% full load (C1:100V/div, C2: 5V/div, t: 100ns/div)

Fig. 24 (a) Turn off of \( S_4 \) (a) with coupled inductor (C1:100V/div, C2: 10V/div, t: 200ns/div) and (b) without coupled inductor at 50% of full load [2] (C1:100V/div, C2: 10V/div, t: 50ns/div)
Overall efficiency of the AC-DC three phase converter is shown in Fig. 27. This efficiency results shown in Fig.27 emphasizes the importance of the proposed load adaptive ZVS approach. Efficiency results of the AC-DC converter with three level DC-DC PWM converter similar to [1]-[3] having non-coupled inductor for ZVS and also efficiency of the AC-DC converter with conventional PWM three level DC-DC converter are also shown. The efficiency requirement of the platinum efficiency standard [28] for different percentages of full load is also shown.

It can be seen that the overall efficiency is higher for the AC-DC converter with proposed DC-DC converter especially in the range of 10% to 100% and especially in the range of 10% to 50% which is important to meet platinum efficiency standards for AC-DC three phase converters for data centers and other similar applications. At around 20% load, the converter losses are predominantly switch losses while at 50%, the losses are both switching and conduction, so it is imperative not to increase the conduction losses too much from the inductive currents required for ZVS of the devices in order to meet such high efficiency values for overall AC-DC converter. This is where the importance of the proposed approach lies. While the non-load adaptive ZVS approach followed in [1]-[3] can barely attain the efficiency requirement at 20% load but it fails to do so at around 50% whereas the proposed approach shows superior performance for all key loads.

From this comparative efficiency graph it can be concluded that the proposed ZVS method is perhaps the only possible optimized load adaptive ZVS technique for achieving platinum efficiency standards in such AC-DC converters with DC-DC PWM converters operating at high switching frequencies of 200 kHz and above.

It should also be noted presently low load and mid load efficiencies of such ac-dc converters are of utmost importance than full load efficiencies since such converters always operate in parallel with similar converters along with load cycling so that at any point of time these converters mostly operate from 20% to 60% of full load. It is this typical load profile of the converter that has enforced agencies like Energy Star to develop such strict efficiency requirements at low and mid loads of a converter. To meet such standards proposed load adaptive ZVS technique is imperative for three level PWM DC-DC converters and herein lays the significance of the proposed ZVS approach with unique magnetic coupling.

V. COMPARATIVE STUDY OF ZVS THREE LEVEL DC-DC CONVERTERS

A comparative study of three level PWM DC-DC converters is presented in this section and in table III. The three converters compared are the regular PWM phase shift three level DC-DC converter, the proposed load adaptive full range ZVS DC-DC three level converter, the converter proposed in [2] and the converter published in [5].

As mentioned earlier, the regular PWM three level converter is the cheapest and simplest converter to implement but at the same time it relies on the energy of the leakage inductor of the transformer for ZVS and hence loses ZVS typically around 60% to 70% of full load. This calls for the need of external assistance for implementing ZVS which is all the more significant to meet efficiency requirements of new efficiency standards [28].
Full load range ZVS three level PWM DC-DC converters have been proposed primarily in [2] and [5] which are used for comparison in table 1. Although the topology in [5] exhibits load adaptive ZVS as claimed in [5] but it alters the basic operation of the three level DC-DC PWM converter so that the primary current is significantly increased and so are the currents in the auxiliary circuit. Moreover the auxiliary inductors require complicated magnetic designing and winding process so that they can be implemented inside the same core as the main power transformer. It should be noted that such converters are mainly implemented with planar cores and such complicated multi winding transformers are difficult to implement in planar cores. Another key drawback of this topology is that the auxiliary circuit is uniquely placed on the path of the transformer primary current which significantly increases the current rating of the flying capacitors and henceforth their cost.

VI. CONCLUSION

Presently strict efficiency standards have been set up to reduce overall energy consumed by loads powered by the utility mains in data centers. In such applications, the power converters mostly operate between 20% of full load and 60% of full load, so higher efficiencies need to be achieved at these low and mid-range loads. To increase efficiency at such load range, load adaptive ZVS must be ensured for whole load range from no load to full-load operation of the dc-dc converter of an AC-DC converter. In this paper a novel yet simple auxiliary ZVS circuit for three-level DC-DC converters is proposed using a uniquely coupled inductor strategically placed in a PWM three-level DC-DC converter. The simple auxiliary circuit gives rise to a load adaptive ZVS. The operation of the proposed converter operation has been extensively discussed, analyzed and validated by experimental results obtained from a laboratory prototype. The load adaptive approach helps the overall three phase AC-DC converter which is a cascaded configuration of front end three phase boost PWM converter and the proposed PWM three level DC-DC isolated converter to conform to Energy Star Platinum Efficiency standard.

REFERENCES


TABLE III

<table>
<thead>
<tr>
<th>Topology</th>
<th>Primary voltage</th>
<th>Primary Current (r.m.s.)</th>
<th>ZVS Range</th>
<th>Number of auxiliary component</th>
<th>Auxiliary inductor size (Volts seconds)</th>
<th>Auxiliary circuit peak current rating</th>
<th>Comparative cost</th>
<th>Complexity</th>
<th>Power Density</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional PWM Topology</td>
<td>$\frac{V_{dc}}{2}$, $0,-\frac{V_{dc}}{2}$</td>
<td>1 p.u.</td>
<td>Typically full load to around 70% full load</td>
<td>None</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td>cheapest</td>
<td>Simplest</td>
<td>Lower than proposed because of low efficiency, hence requires larger heat sinks</td>
</tr>
<tr>
<td>Proposed</td>
<td>$\frac{V_{dc}}{2}$, $0,-\frac{V_{dc}}{2}$</td>
<td>1 p.u.</td>
<td>Load adaptive full load range and assures ZVS turn-off</td>
<td>Three (One coupled Inductor, two film capacitors)</td>
<td>$\frac{V_{dc}}{(1-d_{min})f_{sw}}$</td>
<td>$\frac{V_{dc}(1-D)I_{sw}}{32L_{aux}}$</td>
<td>Cheaper than [2] and [5]</td>
<td>Easier than [2] because less number of components required</td>
<td>Highest amongst conventional, [2], [3] and [5]</td>
</tr>
<tr>
<td>Topology in [2] (published in TPEL)</td>
<td>$\frac{V_{dc}}{2}$, $0,-\frac{V_{dc}}{2}$</td>
<td>1 p.u.</td>
<td>NON-Load adaptive full load range may not assure ZVS turn-off at higher loads</td>
<td>Four (Two auxiliary Inductors, two film capacitors)</td>
<td>$\frac{V_{dc}}{16f_{sw}}$</td>
<td>$\frac{V_{dc}T_{sw}}{32L_{aux}}$</td>
<td>Cheaper than [5]</td>
<td>Easier than [5] since transformer is conventional</td>
<td>Lower than proposed because of additional component count</td>
</tr>
<tr>
<td>Topology in [5] (published in TPEL)</td>
<td>$\frac{V_{dc}}{4}$, $0,-\frac{V_{dc}}{4}$</td>
<td>2 p.u.</td>
<td>Load adaptive full load range and assures ZVS turn-off</td>
<td>Three (One coupled Inductor, two film capacitors)</td>
<td>$\frac{V_{dc}}{(1-d_{min})f_{sw}}$</td>
<td>$I_{a}(t_{a}) + \frac{V_{dc} - NV_{o} DT_{s}}{N^2L_{o} + \frac{I_{a}^2}{2} + \frac{V_{dc}(1-D)I_{sw}}{32L_{aux}}}$</td>
<td>Reflected primary current and the auxiliary circuit current</td>
<td>Costliest since film capacitors have to be very high current rated and requires complex transformer windings</td>
<td>Most complex since special magnetics design has to be done for transformer</td>
</tr>
</tbody>
</table>
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