A Unity Power Factor Correction Bridgeless Isolated-Cuk Converter Fed Brushless-DC Motor Drive

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Abstract—This work presents a power factor correction (PFC) based bridgeless isolated Cuk converter fed brushless DC (BLDC) motor drive. A variable DC link voltage of the voltage source inverter (VSI) feeding BLDC motor is used for its speed control. This allows the operation of VSI in discontinuous inductor current mode (DICM) to achieve an inherent PFC at AC mains. The proposed drive is controlled using a single voltage sensor to develop a cost effective solution. The proposed drive is implemented to achieve a unity power factor at AC mains for a wide range of speed control and supply voltages. An improved power quality is achieved at AC mains with power quality indices within limits of IEC 61000-3-2 standard.

Index Terms— BLDC Motor, Bridgeless Isolated Cuk Converter, Discontinuous Inductor Current Mode, Power Factor Correction, Power Quality, Voltage Source Inverter.

I. INTRODUCTION

ADVANTAGES such as high efficiency, high torque/inertia ratio, high power density, wide range of speed control and low noise and electro-magnetic interference (EMI) make brushless DC (BLDC) motor an ideal choice in many applications [1]. Due to these advantages, BLDC motor finds applications in many household appliances, industrial tools, medical equipments, precise motion control and automation and transportation [1-5]. A BLDC motor consists of a three phase concentrated windings on the stator and permanent magnets on the rotor [1]. A three-phase voltage source inverter (VSI) is used for achieving an electronic commutation of the BLDC motor based on the rotor position as sensed by Hall-Effect position sensors [6].

A VSI fed BLDC motor drive is generally supplied by a combination of a diode bridge rectifier (DBR) with a high value of smoothening DC link capacitor [7]. This combination of DBR and DC link capacitor draws current only for a small duration when the instantaneous value of supply voltage is higher than the DC link voltage [8]. Therefore, a peaky current is drawn from the AC mains, which has very high value of harmonic contents [8]. The total harmonic distortion (THD) of such current is of the order of 60-80 % which leads to a very poor factor (PF) of the order of 0.6-0.7 at AC mains. Such power quality indices are not acceptable under the limits of international power quality standard IEC 61000-3-2 [9].

Extra incurred cost of such drives on sensors is one of the major issues in the development of BLDC motor drives. These current sensors are required for achieving the pulse width modulation (PWM) based current control of BLDC motor for speed control [6, 7]. Moreover, such BLDC motor drives also suffer from high losses in VSI due to high switching frequency. Such losses are reduced by operating the VSI in low frequency switching by electronically commutating the BLDC motor. Moreover, the speed of the BLDC motor is controlled by varying the DC link voltage of the VSI [7]. Such combination provides a twin benefit of reduced switching losses in VSI and an elimination of current sensors for PWM based control of BLDC motor.

Power factor correction (PFC) converters are used to avoid power quality problems at the AC mains and to meet the prescribed guidelines of IEC 61000-3-2 [10, 11]. The sensing requirement of this PFC converter plays major role in deciding the cost of overall system. The required number of sensors for a PFC converter is primarily decided by its mode of operation of the PFC converter. Continuous inductor current mode (CICM) and discontinuous inductor current mode (DICM) are two modes of operation of the PFC converter. In CICM, or continuous conduction mode (CCM), the current in inductor remains continuous in a switching period, whereas the current becomes discontinuous in a switching period for a PFC converter operating in DICM. The PFC converter operating in CICM uses a current multiplier approach for voltage control and power factor correction. It has lower current stress on the PFC converter switch but requires three sensors (2-V, 1-C) for its operation. However, a single voltage sensor is used for a PFC converter operating in DICM using voltage follower approach, but at the cost of high current stress on the PFC converter switches [12]. Therefore, this mode of operation is suited for low power applications.

Manuscript received April 14, 2014; revised July 3, 2014 and September 12, 2014; accepted September 28, 2014.

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A conventional boost-PFC converter has been widely used for power quality improvements at AC mains [13, 14]. This converter has also been used at the front-end of a VSI feeding BLDC motor for power factor correction at AC mains [15-16]. Such configuration maintains a constant DC link voltage of the VSI and controlling the speed of BLDC motor by using a PWM based switching of VSI. These configurations suffer from high switching losses in VSI due to high switching frequency of PWM signals and high cost associated due to large numbers of sensors. An overview of such configurations has been presented in [17], but these also suffer from high switching losses. A variable voltage controlled single ended primary inductance converter (SEPIC) has also been presented in [18], but it also uses a PWM based control of BLDC motor. A review of these PFC topologies for brushless DC motor drives has been presented in [19].

Bridgeless PFC converters have gained attention due to lower conduction losses in the front end converter by partial or complete elimination of the front-end DBR [20-33, 36-38]. The bridgeless buck and boost PFC converters have been reported in [20] and [21], but have a limited voltage conversion ratio (ratio between output and input voltage) i.e. < 1 for buck and > 1 for boost converter. Therefore, these converters cannot be used for wider range of DC link voltage control. A bridgeless buck-boost converter feeding BLDC motor drive has been presented in [22], but it doesn’t provide high frequency isolation. A non-isolated configuration of bridgeless Cuk converter has been presented in [23-26]. These configurations are derived from the non-isolated Cuk Converter. Similarly, bridgeless configurations of a SEPIC, Zeta and canonical switching cell (CSC) converters have been presented in [27], [28] and [29] respectively for improving the power quality at AC mains. These configurations present non isolated converter, which cannot be used in applications requiring galvanic isolation such as refrigerators.

Bridgeless configurations of PFC based flyback converter have been proposed in [30-32]. These converters have low component count but find applications in very low power rating, ranging up to 100-150 W. A bridgeless isolated-Cuk converter has also been proposed in [33] which is derived from the isolated Cuk converter [34, 35]. Bridgeless configurations of SEPIC and Zeta converters with high frequency isolation have also been presented in [36-37] and [38] respectively.

Table-I shows a comparison of various bridgeless PFC converter configurations. This comparison is made on the basis of number of components, conducting components during half period of line cycle, suitability to variable voltage applications, high frequency isolation and complexity of the gate drivers. Many of these configurations require high-low side and isolated gate driver circuits. The high low side gate drivers use bootstrap circuits for gating two solid-state switches of the PFC converter. Moreover, the isolated gate drivers use pulse transformers for isolating two gate pulses for two solid-state switches of the PFC converter. Therefore, these features increase the cost and the complexity of gate drivers.

However, the proposed PFC bridgeless isolated-Cuk converter uses a low side gate driver which is simple in design and a single gate driver can also be used to trigger both solid-state switches of the PFC converter at same instant.

II. PROPOSED PFC BRIDGELESS ISOLATED-CUK CONVERTER FED BLDC MOTOR DRIVE

Fig. 1 shows the proposed PFC bridgeless isolated-Cuk converter fed BLDC motor drive. A single-phase supply followed by a LC-filter is used to feed a bridgeless isolated-Cuk converter. This maintains the required DC link voltage of the VSI and provides power factor correction at AC mains. The proposed PFC converter is designed to operate in DICM to act as an inherent power factor corrector. The DC link voltage of the VSI is controlled for adjusting the speed of the BLDC motor. The VSI feeding the BLDC motor is operated in a low frequency switching to achieve an electronic commutation of BLDC motor for reduced switching losses. The proposed configuration uses a single voltage sensor to control the DC link voltage for speed control of BLDC motor. The proposed drive is designed and its performance is validated on a developed prototype for improved power quality at AC mains for a wide range of speed control and supply voltages. Specifications of a BLDC motor selected for experimental studies are given in Appendix-A.
III. OPERATION OF PFC BASED BRIDGELESS ISOLATED-CUK CONVERTER

The operation of proposed PFC converter is classified into two different sections for a line cycle and a switching cycle. Fig. 2 shows six different modes of operation. Moreover, Fig. 3 shows the associated waveforms of the PFC converter during a complete switching period.

A. Operation during Complete Line Cycle of Supply Voltage

The proposed bridgeless isolated-Cuk converter is designed such that switches $S_{m1}$ and $S_{m2}$ conduct for positive and negative half cycles of supply voltage respectively. During the positive half cycle of supply voltage, switch $S_{m1}$, inductors $L_{m1}$ and $L_{m2}$, intermediate capacitors $C_{m1}$ and $C_{m2}$ and diodes $D_{m1}$ and $D_{m2}$ are in state of conduction and vice-versa for negative half cycle of supply voltage as shown in Figs. 2 (a-f). As shown in these figures, the proposed PFC converter operates in three different modes during the positive and negative half cycles of the supply voltage. Moreover, during the DICM operation, the current of output inductors ($L_{m1}$ and $L_{m2}$) becomes discontinuous in a switching period. However, the current flowing in input and magnetizing inductance of HFT ($L_{m1}$) and ($L_{m2}$) voltage across the intermediate capacitor ($C_{m1}$, $C_{m2}$, $C_{m1}$ and $C_{m2}$) remain continuous in a complete switching period.

B. Operation during Complete Switching Cycle

Figs. 2 (a-c) show three modes of operation of a bridgeless isolated-Cuk converter in a switching period for positive half cycle of supply voltage. Fig. 3 shows its associated waveforms in DICM ($L_{o}$) mode of operation as follows.

Mode P-I: In this mode, when switch ($S_{m1}$) is turned-on, the input inductor ($L_{o1}$), output inductor ($L_{o2}$) and magnetizing inductance of high frequency transformer (HFT) ($L_{m1}$) start charging as shown in Fig. 2 (a). The input side intermediate capacitor ($C_{i1}$) supplies the energy to the HFT and output side intermediate capacitor ($C_{m1}$) supplies the required energy to the DC link capacitor as shown in Fig. 3.

Mode P-II: When switch ($S_{m1}$) is turned-off, input inductor ($L_{o1}$), output inductor ($L_{o2}$) and magnetizing inductance of HFT ($L_{m1}$) start discharging as shown in Fig. 2 (b). The intermediate capacitors ($C_{i1}$ and $C_{m1}$) charge and the DC link capacitor ($C_{o}$) discharges in this interval as shown in Fig. 3.

Mode P-III: During this interval, the output side inductor ($L_{o1}$) is completely discharged and the input inductor ($L_{o1}$) and magnetizing inductance of HFT ($L_{m1}$) continue to discharge as shown in Fig. 2(c). The output side intermediate capacitor ($C_{m1}$) continues to charge and the DC link capacitor ($C_{o}$) supplies the required energy to BLDCM as shown in Fig. 3.

In a similar way, the operation for the negative half cycle of the supply voltage is realized.

Initially, the intermediate capacitors ($C_{i1}$, $C_{i2}$, $C_{m1}$ and $C_{m2}$) are completely discharged and are charged during the operation of the PFC converter. The voltage across the input side intermediate capacitors ($C_{i1}$ and $C_{i2}$) depends upon the instantaneous input voltage; hence, the initial charging of $C_{i1}$ and $C_{i2}$ is zero. However, the output side intermediate capacitors ($C_{m1}$ and $C_{m2}$) are not completely discharged in a switching period or a half line cycle of supply voltage due to the voltage maintained at the DC link capacitor ($C_{o}$).

Moreover, during the operation of PFC converter in positive half cycle; the energy storage components on the primary side of the HFT (i.e. $L_{o1}$, $C_{i1}$ and $L_{m2}$) remain in non-conducting state and are completely discharged. However, the energy storage components on the secondary side of HFT (i.e. $C_{m1}$) remain charged at its full voltage due to the unavailability of discharging path and the presence of DC link capacitor ($C_{o}$).

IV. DESIGN OF BRIDGELESS ISOLATED-CUK CONVERTER

A bridgeless isolated-Cuk converter is designed to operate in DICM such that the current flowing in the output inductors...
(L_{o1} and L_{o2}) becomes discontinuous in a switching period. A PFC converter of 250 W ($P_{\text{max}}$) is designed for the selected BLDC motor (Specifications given in Appendix). For a wide range of speed, the DC link voltage is controlled from 50 V ($V_{\text{dcmin}}$) to rated voltage of 130 V ($V_{\text{dcmax}}$) with supply voltage variation from 170 V ($V_{\text{smi}}$) to 270 V ($V_{\text{smax}}$).

The input voltage, $v_s$ applied to the PFC converter as,

$$v_s(t) = V_m \sin(2\pi f_L t) = 220\sqrt{2} \sin(314t)$$

where $V_m$ is peak input voltage (i.e. $\sqrt{2}V_S$), $f_L$ is line frequency i.e. 50 Hz.

Now, the instantaneous value of rectified voltage is as,

$$V_{\text{in}}(t) = |V_m \sin(\omega t)| = |220\sqrt{2} \sin(314t)|$$

where $|$ represents the modulus function.

The output voltage, $V_{\text{dc}}$ of a bridgeless isolated-Cuk converter which is a buck-boost configuration is given as [11],

$$V_{\text{dc}} = \left( \frac{N_2}{N_1} \right) \frac{D}{(1-D)} V_{\text{in}}$$  \hspace{1cm} (3)

where $D$ represents the duty ratio and $(N_2 / N_1)$ is the turns ratio of the HFT which is taken as $1/2$ for this application.

The instantaneous value of duty ratio, $D(t)$ depends on the input voltage and DC link voltage. Instantaneous duty ratio, $D(t)$ is obtained by substituting (2) in (3) and as,

$$D(t) = \frac{V_{\text{dc}}}{(N_2 / N_1)V_{\text{in}}(t) + V_{\text{dc}}} = \left( \frac{N_2 / N_1}{V_{\text{dc}}} \right) \frac{V_{\text{dc}}}{|V_m \sin(\omega t)|} + V_{\text{dc}}$$  \hspace{1cm} (4)

Since the speed of BLDC motor is controlled by varying the DC link voltage of VSI, therefore the instantaneous power, $P_i$ is taken as linear function of $V_{\text{dc}}$ as,

$$P_i = \left( \frac{P_{\text{max}}}{V_{\text{dcmax}}} \right) V_{\text{dc}}$$  \hspace{1cm} (5)

Fig. 2. Different modes of operation of bridgeless isolated Cuk converter during positive (a-c) and negative (d-f) half cycle of supply voltage.
The maximum current ripple in an inductor occurs at the maximum power and at minimum value of supply voltage (i.e. \( V_{\text{min}} \)). Hence the output inductor is calculated at the peak of supply voltage (i.e. \( V_{\text{in}} = \sqrt{2}V_{\text{min}} \)).

The critical value of output side inductors is calculated at the minimum \( (L_{\text{oc},50}) \) and maximum \( (L_{\text{oc},120}) \) values of DC link voltages using (7) as 459.79 \( \mu \text{H} \) and 811.93 \( \mu \text{H} \) respectively. Hence, the critical value of output inductor is selected lower than minimum value i.e. \( L_{\text{oc},50} \) to ensure a discontinuous conduction even at lower values of DC link voltages [39]. Therefore, the output inductor \( (L_{\text{o1}}, L_{\text{o2}}) \) of 70 \( \mu \text{H} \) is selected for its operation in discontinuous conduction.

The value of magnetizing inductance of HFT to operate in CICM is decided by the permitted ripple current (\( \xi \)) as [11],

\[
L_{\text{m1,2}} = \frac{V_{dc}}{\Delta I_{Lm}(t)\eta f_S} = \left( \frac{V_S^2}{P_i} \right) \left( \frac{1}{\sqrt{2} f_S n V_{\text{in}}(t) + V_{dc}} \right) \tag{8}
\]

The maximum current occurs at maximum DC link voltage (i.e. \( P_{\text{max}} \)) and the minimum supply voltage (i.e. \( V_{\text{min}} \)).

Therefore, the value of magnetizing inductance \( (L_{\text{o1}}, L_{\text{o2}}) \) for a permitted ripple current (\( \xi \)) of 50% is calculated using (8) as 6.006 mH and is selected as 6 mH.

The value of input side intermediate capacitors to operate in CCM with a permitted ripple voltage of \( \kappa \% \) of \( V_{C1} \) is as [11],

\[
C_{11,12} = \frac{V_{\text{in}}^2}{\Delta V_{C1}(t) R_L f_S} \left( \frac{1}{\xi} \frac{1}{n f_S} \right) \left( \frac{V_{dc}}{n V_{\text{in}}(t) + V_{dc}} \right) \tag{9}
\]

The input side intermediate capacitors \( (C_{11} \text{ and } C_{12}) \) are calculated at maximum value of voltage ripple corresponding to maximum supply voltage \( (V_{\text{max}}) \) and at rated DC link voltage. Now, for a permitted ripple voltage of 25%, the value of \( C_{11} \) and \( C_{12} \) are calculated using (9) as 204 nF and are selected as 220 nF.

The value of output side intermediate capacitors to operate in CCM with permitted ripple voltage of \( \chi \% \) of \( V_{C2} \) is as [11],

\[
C_{21,22} = \frac{V_{dc}}{\Delta V_{C2}(t) R_L f_S} = \frac{P_i}{\chi V_{dc} f_S} \left( \frac{n V_{dc} \sqrt{2 V_s} + V_{dc}}{n V_{dc} \sqrt{2 V_s} + V_{dc}} \right) \tag{10}
\]

The maximum ripple voltage occurs at rated condition and at maximum value of DC link voltage \( (V_{\text{max}}) \). Hence the output side intermediate capacitor \( (C_d) \) is calculated at maximum permitted ripple voltage of 10% (\( \gamma \)) of \( V_{C21,22} \) at maximum \( (C_{d270}) \) and minimum \( (C_{d2170}) \) value of supply voltage as 2.99 \( \mu \text{F} \) and 3.84 \( \mu \text{F} \) respectively. Therefore, the output side intermediate capacitors \( (C_{d1}, C_{d2}) \) are selected higher than \( C_{d270} \) of the order of 4.4 \( \mu \text{F} \).

The value of DC link capacitor \( (C_d) \) is calculated as [11],

\[
C_d = \frac{1}{2 \alpha V_{dc}} \left( \frac{P_i}{V_{dc}} \right) \frac{1}{2 \alpha (\rho V_{dc})} \tag{11}
\]
where \( \Delta V_{\text{dc}} \) represents the permitted ripple in DC link voltage.

The worst case design occurs for the minimum value of DC link voltage i.e. 50 V. Hence, for a permitted ripple voltage of 3% (\( \rho \)), the value of DC link capacitor is calculated using (11) as 20.38 mF and it is selected as 2200 \( \mu \)F.

A low pass LC filter is used to avoid the reflection of higher order harmonics in the supply system. The maximum value of filter capacitance (\( C_{\text{max}} \)) is given as [40],

\[
C_{\text{max}} = \frac{I_m}{\omega I V_m} \tan(\theta) = \left( \frac{P_{\text{max}} \sqrt{2}/V_s}{\omega L \sqrt{2V_s}} \right) \tan(\theta) \tag{12}
\]

where \( \theta \) is the displacement angle between fundamental value of supply voltage and supply current and is taken as 2\(^\circ\).

The maximum value of filter capacitor is calculated using (12) as 574.4 nF and is selected as 330 nF.

The value of filter inductor is designed by considering the source impedance (\( L_s \)) of 4-5% of the base impedance. Hence the additional value of inductance required is given as,

\[
L_f = L_{\text{req}} + L_s \Rightarrow L_{\text{req}} = L_f - L_s
\]

\[
\therefore L_{\text{req}} = \frac{1}{4\pi^2 f_c^2 C_f} \cdot 0.025 \left( \frac{1}{\omega L_s} \right) \left( \frac{V_s^2}{P_o} \right) \tag{13}
\]

where \( f_c \) is the cut-off frequency which is selected such that \( f_L < f_c < f_s \). Therefore \( f_c \) is taken as \( f/s/10 \).

Hence the value of filter inductance is calculated using (13) as 3.77 mH.

V. CONTROL OF PFC BRIDGELESS ISOLATED-CUK CONVERTER FED BLDC MOTOR DRIVE

The control of proposed BLDC motor drive is divided into two categories of control of PFC converter for DC link voltage control and control of three-phase VSI for achieving the electronic commutation of BLDC motor as follows.

A. Control of Front-End PFC Converter

A voltage follower approach is used for the control of PFC based bridgeless isolated-Cuk converter operating in DCM. This control scheme consists of a reference voltage generator, voltage error generator, voltage controller and a PWM generator. A ‘Reference Voltage Generator’ generates a reference voltage \( V_{dc^*} \) by multiplying the reference speed (\( \omega^* \)) with the motor’s voltage constant (\( k_v \)) as,

\[
V_{dc^*} = k_v \omega^* \tag{14}
\]

The ‘Voltage Error Generator’ compares this reference DC link voltage (\( V_{dc^*} \)) with the sensed DC link voltage (\( V_{dc} \)) to generate an error voltage (\( V_e \)) given as,

\[
V_e(k) = V_{dc^*}(k) - V_{dc}(k) \tag{15}
\]

where ‘\( k \)’ represents the \( k^{th} \) sampling instance.

This error voltage, \( V_e \), is given to a voltage PI (Proportional-Integral) controller to generate a controlled output voltage (\( V_{cc} \)) which is expressed as,

\[
V_{cc}(k) = V_{cc}(k-1) + K_p \left[ V_e(k) - V_e(k-1) \right] + K_i V_e(k) \tag{16}
\]

where \( K_p \) and \( K_i \) are the proportional and integral gains of the PI controller (values given in Appendix).

Finally the PWM signals for switch \( S_{w1} \) and \( S_{w2} \) are generated by comparing the output of PI controller (\( V_{cc} \)) with high frequency saw-tooth signal (\( m_d \)) given as,

\[
\begin{align*}
For V_S > 0: & \quad \text{if } m_d < V_{cc} \text{ then } \text{PWM}_{Sw1} = \text{‘ON’} \quad (17) \\
& \quad \text{if } m_d \geq V_{cc} \text{ then } \text{PWM}_{Sw1} = \text{‘OFF’} \\
For V_S < 0: & \quad \text{if } m_d < V_{cc} \text{ then } \text{PWM}_{Sw2} = \text{‘ON’} \\
& \quad \text{if } m_d \geq V_{cc} \text{ then } \text{PWM}_{Sw2} = \text{‘OFF’}
\end{align*}
\]

where PWM\(_{Sw1} \) and PWM\(_{Sw2} \) represent the gate signals to PFC converter switches \( S_{w1} \) and \( S_{w2} \) respectively.

In this control algorithm, (17) shows the solid-state switches of the PFC converter operating at half cycles of supply voltages. However, to avoid the sensing of supply voltage for zero crossing detection (ZCD), only one PWM signals is generated to drive both solid-state switches of the PFC converter i.e. PWM\(_{Sw1} = \text{PWM}_{Sw2} \). Moreover, the PFC converter is operating in DCM, therefore, the input current shaping in phase with the supply voltage is obtained inherently and a unity power factor is achieved at the AC mains [11].

B. Control of BLDC Motor: Electronic Commutation

An electronic commutation of the BLDC motor includes proper switching of the VSI in such a way that a symmetrical DC current is drawn from the DC link capacitor for 120\(^\circ\) and is placed symmetrically at centre of back-EMF of each phase [22]. A Hall-Effect position sensor is used to sense the rotor position on a span of 60\(^\circ\), which is required for electronic commutation of the BLDC motor. As shown in Fig. 1, when two switches of the VSI i.e. \( S_1 \) and \( S_2 \) are in conducting states, a line current \( i_{ab} \) is drawn from the DC link capacitor which magnitude depends on the applied DC link voltage (\( V_{dc} \)), back-EMF’s (\( e_{ia} \) and \( e_{ib} \)), resistances (\( R_a \) and \( R_b \)) and self and mutual inductance (\( L_{oa}, L_{ob} \) and \( M \)) of stator windings [22]. This current produces an electromagnetic torque (\( T_e \)) which in-turn increases the speed of the BLDC motor.

VI. RESULTS AND DISCUSSION

The performance of the proposed BLDC motor drive is validated on a developed hardware prototype. A digital signal processor (DSP- Texas Instruments TMS320F2812) is used for the development of the proposed drive. An opto-isolation is provided between DSP and gate driver of the VSI and PFC converter switches. Hall signal filtering and power circuitries are also developed for Hall Effect position sensors. Moreover, a DSP based moving average filter (MAF) is also designed for Hall signal filtering to obtain an improved rotor position sensing for satisfactory operation of BLDC motor [41]. Test results of the proposed BLDC motor drive obtained on a developed prototype are discussed as follows.
A. Steady State Performance of Proposed Drive

Figs. 4 (a) and 4 (b) show the test results of the proposed BLDC motor drive operating at rated load with supply voltage as 220 V and DC link voltage of 130 V and 50 V respectively. As shown in these figures, the DC link voltage is maintained at desired reference value and different magnitude and frequency of the stator current demonstrate the operation of BLDC motor at different speeds. A sinusoidal supply current in phase with supply voltage is obtained which shows a near unity power factor at both values of DC link voltages. The obtained power quality indices at the AC mains in both the mentioned cases are discussed in sub-section C.

B. Performance of PFC Bridgeless Isolated-Cuk Converter

Figs. 5 (a), 5 (b) and 5 (c) show the current in input inductors ($i_{Li1}$, $i_{Li2}$), output inductors ($i_{Lo1}$, $i_{Lo2}$) and high frequency transformer ($i_{HFT,p}$ and $i_{HFT,s}$) respectively. A continuous current in the input inductors and a discontinuous current in the output inductors are achieved, which confirms the DICM operation of the PFC converter. As shown in these figures, alternate inductors are conducting in a half line cycle of supply voltage, which confirms the bridgeless operation of the PFC converter. Moreover, the continuous voltage across the input and output side intermediate capacitors is achieved as shown in Figs. 6 (a) and 6 (b) respectively.

The template of voltage and current of the PFC converter switch and its enlarged waveform are shown in Figs. 7 (a) and 7 (b) respectively. A peak voltage and current stresses of 680 V and 19 A are observed as shown in Fig. 7 (b); which is acceptable for a PFC converter operating in DICM. Moreover, as shown in Figs. 7 (a) and 7 (b), the current in the PFC converter switches flows for a half cycle of supply voltage; therefore, the rms current flowing in the switch also reduces to half. This reduces the conduction losses in the individual solid
state switch of PFC converter. Hence, the heat dissipation corresponding to such reduced conduction losses is also very low which leads to a lower size of heat sink required per switch. However, two switches are required for the bridgeless PFC converter which require two heat sinks; hence, the size of the PFC converter increases. Moreover, single diode (either \( D_p \) or \( D_n \)) is conducting in each half line cycle of the supply voltage, hence the conduction losses as compared to the DBR are also reduced.

C. PFC and Improved Power Quality at AC Mains

This section deals with the obtained power quality indices at AC mains for the operation of the proposed BLDC motor drive at different values of DC link voltages and supply voltages. A power analyzer (‘Fluke’ make) is used for the measurement of power quality indices at AC mains. Various power quality indices are obtained from three different types of recorded waveforms. First set of waveform of four different cases (Figs. 8 (a), (d), (g), (j)) show the root mean squared (RMS) value, frequency and the crest factor (CF) of supply voltage and supply current, respectively. The second set of waveforms (Figs. 8 (b), (e), (h), (k)) show the active, reactive and apparent powers, power factor (PF) and displacement power factor (DPF) at AC mains. Moreover, the third set of waveforms (Figs. 8 (c), (f), (i), (l)) show the harmonic spectra and the obtained THD of supply current at AC mains.

Figs. 8 (a-c) and (d-f) show the performance of proposed drive at rated supply voltage with a DC link voltage as 130 V and 50 V respectively. A near unity power factor is achieved at the AC mains in both the cases as shown in Fig. 8 (b) and Fig. 8 (e). Moreover, Figs. 8 (g-i) and (j-l) show performances at rated DC link voltage and rated load on the BLDC motor with supply voltages as 170 V and 270 V respectively. An improved power quality is achieved at AC mains satisfying IEC 61000-3-2 [9].

D. Dynamic Performance of Proposed Drive

Fig. 9 shows the dynamic performance of the proposed BLDC motor drive at starting, speed control and supply voltage fluctuations. Fig. 9 (a) shows the performance of proposed BLDC motor drive during starting at DC link voltage of 50 V. A limited inrush current within the maximum current limit of the stator windings is drawn from the DC link capacitor and the supply system. Fig. 9 (b) shows the dynamic performance during speed control corresponding to step change in DC link voltage from 50 V to 100 V. Moreover, the dynamic behavior of the proposed drive during supply voltage fluctuations corresponding to step change in supply voltage from 250 V to 200 V is shown in Fig. 9 (c). A smooth variation of the DC link voltage with limited stator current is obtained in all these cases which demonstrate a satisfactory performance of the proposed BLDC motor drive.
E. Comparison of Efficiency of Proposed PFC Converter with PFC Boost-Flyback Converter

The measured efficiency of the proposed bridgeless isolated-Cuk converter is evaluated at different values of DC link voltages, supply voltages and loading conditions. Moreover, the efficiency of this bridgeless PFC converter is also compared with the two-stage boost-flyback converter. The circuit configuration of a boost-flyback converter is shown in Fig. 10. This converter consists of a PFC boost converter operating in DCM followed by a flyback DC-DC converter operating in CCM. Fig. 11 (a) shows the efficiency of the proposed bridgeless isolated Cuk converter and boost-flyback converter at different values of DC link voltages with load resistance kept at a fixed value of 67.6 Ω. Moreover, Figs. 11 (b) and 11 (c) show the efficiency at two different DC link voltages of 130 V and 50 V for varying supply voltages and load. As shown in these figures, the efficiency of a boost-flyback converter is little higher as compared to the proposed bridgeless isolated Cuk converter due to low number of components conducting during a line cycle. However, two stages in the boost-flyback PFC converter have to be controlled individually for DC link voltage control and maintaining the desired unity power factor at the AC mains. This increases the cost on account of two voltage sensors required for power factor correction and DC link voltage control respectively and thus, increasing the overall complexity of the system.

F. Comparative Analysis of Proposed Drive

This section deals with a comparative study of three configurations of BLDC motor drive. The proposed configuration is compared with a conventional DBR fed BLDC motor drive and a conventional single-switch PFC converter feeding BLDCM drive via a PWM based switching of VSI. Fig. 12 (a) shows the losses in different sections of the conventional schemes and the proposed BLDC motor drive and Fig. 12 (b) shows the efficiency comparison. The losses in VSI of the two conventional schemes are higher on account of its operation at high frequency switching which results in higher switching losses. However, due to losses in PFC converter; total losses of the proposed drive are higher as compared to DBR fed BLDC motor drive. But, power factor correction and improved power quality operation cannot be achieved in such BLDC motor drive fed by a DBR and therefore not a recommended solution. Moreover, both conventional and proposed scheme with PFC give a good power quality performance. However, the conventional scheme has a low efficiency due to high switching losses in PWM based switching of the VSI feeding BLDC motor.
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2014.2384001, IEEE Transactions on Industrial Electronics

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Table-II presents a comparative evaluation of the proposed configuration with the conventional scheme of BLDC motor drive. This evaluation is based on the control requirements, sensor requirements and losses in PFC converter and VSI fed BLDC motor. The proposed configuration requires a single voltage sensor and a simple control loop for DC link voltage control; therefore, a low cost processor can be used for the development purpose. Moreover, the BLDC motor is operated in electronic commutation; hence, two current sensors required for current control in the conventional schemes are also eliminated in the proposed configuration. This further reduces the overall cost of the BLDC motor drive system.

Moreover, higher efficiency due to lower switching losses in the VSI, requirement of minimum sensing and a much simple approach of speed control at reduced cost makes the proposed drive an ideal choice for low power applications.

VII. CONCLUSION

A new configuration of bridgeless isolated-Cuk converter fed BLDC motor drive has been proposed for low power household appliances. The speed control of BLDC motor has been achieved by controlling the DC link voltage of VSI feeding BLDC motor. This has facilitated the operation of VSI in low frequency switching mode for reducing the switching losses associated with it. This bridgeless isolated-Cuk converter has been designed for the elimination of diode bridge rectifier at the front-end for reducing the conduction losses in the front-end converter. This PFC converter has been operated in DICM for DC link voltage control and inherent power factor correction is achieved at the AC mains. A prototype of proposed drive has been implemented using a DSP. Satisfactory test results for proposed bridgeless isolated-Cuk-converter fed BLDC motor has been evaluated for its operation over complete speed range. Moreover, the performance of proposed drive is also evaluated for operation

![Fig. 10. Circuit configuration of a two-stage boost-flyback converter.](image)

![Fig. 9. Test results of the proposed drive during (a) starting at DC link voltage of 50V, (b) speed control corresponding to change in DC link voltage from 50V to 100V and (c) supply voltage fluctuation from 250V to 200V.](image)

![Table II: COMPARATIVE ANALYSIS OF PROPOSED CONFIGURATION WITH CONVENTIONAL SCHEMES](table)
Fig. 11. Efficiency of the proposed PFC based bridgeless isolated-Cuk converter at various values of (a) DC link voltage (b) supply voltages and (c) different loading conditions. \( V_{dc} = 130 \text{ V and 50 V fixed} \)

at wide range of supply voltages. The obtained power quality indices have been found within the limits of international power quality standards such as IEC 61000-3-2.

**APPENDICES**

A. Specifications of BLDC Motor

No. of poles (p): 4, Rated DC bus voltage \( (V_{dc}) \): 130 V, Rated speed \( (\omega_r) \): 1500 rpm, Rated torque \( (T_{rated}) \): 1.2 Nm, Rated Power \( (P_{rated}) \): 188.49 W, Voltage Constant \( (k_V) \): 57.59 V (peak-peak)/krpm, Torque constant \( (k_t) \): 0.55 Nm/A (peak-peak), Stator per phase resistance and inductance \( (R_{ph}, L_{ph}) \): 4.32 \( \Omega \), 8 mH, Moment of Inertia \( (J) \): 1.8 kg-cm².

Fig. 12. Comparison of (a) losses at various stages of BLDC motor drive and (b) efficiency of the proposed PFC based BLDC motor drive with conventional techniques.

B. Controller Gains and Parameters

Proportional Gain \( (K_p) \): 0.3, Integral Gain \( (K_i) \): 0.001, Gain margin \( (GM) \): 86 dB, Phase Margin \( (PM) \): 42.5° and Band-width \( (BW) \): 3.6 rad/sec.

**REFERENCES**

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