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Digitalized-Management Voltage-Domain Programmable Mechanisms for Dual-Vdd Low-Power Embedded Digital Systems

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Abstract

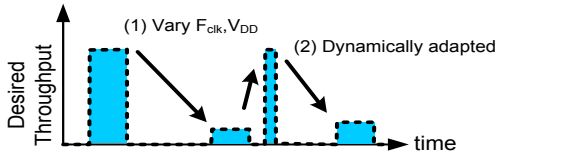
A built-in digitalized power management (DPMM) and voltage domain programmable (VDP) mechanisms are proposed to design a low-power system. In the proposed techniques, the high and low voltages applied to logic modules can be switchable. This flexible voltage-domain assignment allows the chip performance and power consumption can dynamically adjust during circuit operation. To support the DPMM and VDP mechanisms, the voltage-level monitor circuit and power-switch circuit are designed to support multiple operation modes for DPMM-VDP digital circuit designs. A powerless retention flip-flop is developed for temporary data storage during voltage domain dynamically switching. While to prevent the system failure come from voltage integrity problem, a built-in voltage-level monitoring mechanism is utilized to monitor voltage integrity during VDP circuit operation. The proposed mechanism allows the chip performance and power consumption to be flexibly adjusted during circuit operation. The physical implementation chips and measured results proof of this methodology has 30~55% power reduction comparisons with using single-Vdd.

Keywords: power management, voltage domain programmable

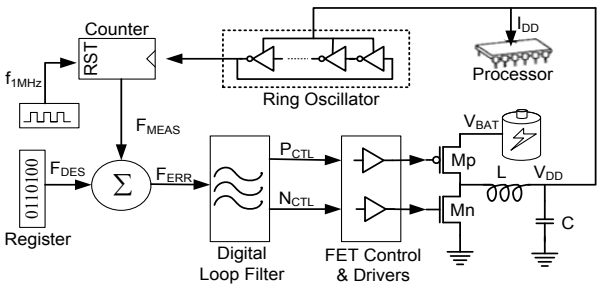
1. Introduction

The conventional Dynamic Voltage Frequency Scaling (DVFS) technique [1] uses a single power source and adjusts the supply voltage level, which simultaneously degrades the circuit power consumption and performance. Figure 1 shows the DVFS system-performance management concept and the utilized mechanism for a circuit. In the DVFS system, all gates use the same voltage level. The power thus wasted for those gates are not in the critical paths. Moreover, as using lower supply voltage, it is possible to lead chip's performance is degraded, due to those gates in the critical paths [2].

The utilization of DVFS technique is limited for an embedded system (e.g., IoT sensor) when single-power voltage-level is degraded to lower than a certain voltage level, the circuit will malfunction. Moreover, when the circuit is going into sleep mode, the supplied voltage needs always maintained, cannot power-off even in a short circuit's function turn-off (sleep-mode) state.



(a) VFS adapts voltage and frequency from the throughput.



(b) Dynamic voltage frequency scaling (DVFS) mechanism.

Fig. 1. The conventional voltage frequency scaling system.

In [8], a fully integrated power delivery system with distributed on-chip low-dropout (LDO) regulators developed for voltage regulation in portable devices and fabricated in a 28 nm CMOS process is proposed. Each LDO employs adaptive bias for fast and power efficient voltage regulation, exhibiting quite-high response time and current efficiency.

In [5], a single battery charging without additional energy harvesting in this design. A die-stacked sensor platform composed of an ARM Cortex M0 processor, energy harvester, power management unit, solar cell, optical receiver, sensor layer, and RF transmitter to exploit ultra-low power operation.

The most different of the proposed technique with the above current methodologies, the proposed low-power methodology is integrated both of the internal chip design with external power managed mechanisms. For the long-life battery-operated system, the availability of DVFS technique is limited, when battery's voltage-level is degraded to lower than a certain voltage level. The circuit will malfunction and the battery must be replaced.

For much embedded digital designs (e.g. IoT sensing circuit), both requirements are essential, High-performance for the circuit in the active mode, while the low-power for the circuit in the monitoring mode. In the circuit active mode, it also depends on the sensing object to decide the system performance for maintaining long-time operation. For example, the surveillance sensing image processor will maintain low-performance operation without object motion.

As the voltage-domain can be re-programmable, with this flexibility to allow the proposed dual-voltage (Dual-Vdd) adjustable design can gain on power-performance digitalize-adaptable system. The proposed technique is more efficient than the DVFS for single-Vdd circuit by a complicate performance-power manageable mechanism, especially for generic embedded systems.

In this paper, the dual-voltage and voltage management techniques are proposed for reducing power consumption, as shown in Figure 2. The proposed voltage domain switching mechanism allows the design module changes the supplied voltage source dynamically during circuit operation. This means high voltage (VddH) or low-voltage (VddL) can charge designed logic modules, dynamically. The altered mechanism is dependent on performance-power planning by the system designers.

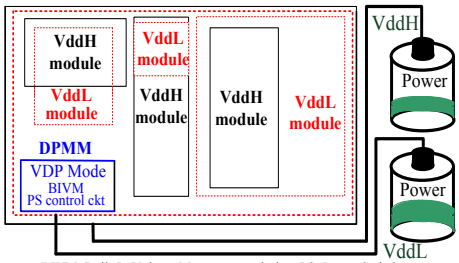


Fig. 2 Proposed Dual-Vdd power-performance manageable design.

When a deigned module works in performance-driving operational mode, there is VddH supply to the designed module. When the module is working in power-saving mode, the voltage-altered technique is switched to VddL to reduce the dynamic power reduction. When the chip works in power-saving mode, there is VddL supply to the more designed module. As the retention flip-flops are utilized within the designed circuit. When a supplied voltage is switching from VddH to VddL, circuit's functions are normal, even without power supplied in a transition moment.

The proposed Module-Level Voltage Domain Programmable (VDP) technique is introduced in the paper [3]. A built-in voltage measurement mechanism (BIVM) [6, 7] is proposed for real-time internal-chip voltage integrity observation.

Although the VDP and BIVM papers have been published. However, there are without the consideration of the voltage integrity issue by physical circuitries for practical implementation. The main contribution of the paper is that the presentation of system design, a real emphasis on the design circuitries to support dynamically switching operation.

This proposed framework includes the integration of digitalized power management (DPMM) mechanism and considers the systemic methodology to implement VDP, while the control circuitry.

The widely DVFS uses voltage regulators to enable multi-voltage system operation from a single power supply. When comparing the proposed Dual-Vdd VDP system with DVFS, the proposed VDP systems are better in terms of area, performance, and energy. Especially, VDP has less-complicate overhead as voltage-domain can be easily reprogrammable. For a low-power embedded system, the dual-Vdd VDP design can gain the most efficient on managing power-performance than a single-Vdd system with DVFS.

These mechanisms are validated by two designed chips and show 30~55% power reduction with a good performance-power manageable characteristic for the low-power design embedded system.

2. The Proposed Digital Low-Power Management Mechanism for Chip Performance Adjustment

An all-digital power aware performance management mechanism is proposed. Figure 3 shows the structural view of the proposed built-in digitalized power management (DPMM) mechanism. Compared with the conventional DVFS technique, DPMM uses the power supply combinations from the two batteries for a longer operation time without additional power management chips. The two batteries, one is high-voltage (VddH), the other is low-voltage (VddL). The proposed DPMM design is easily integrated with the core design within a single die.

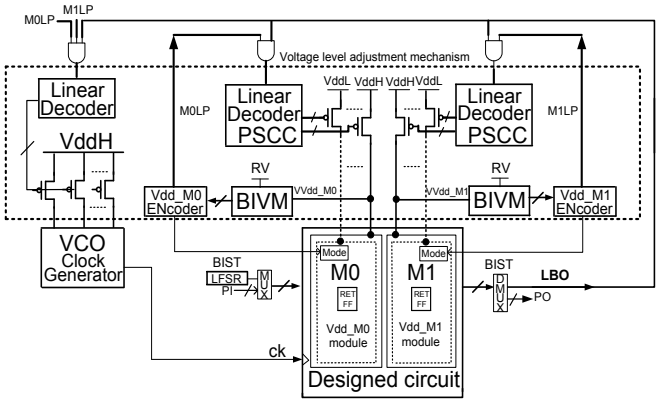


Fig. 3 The proposed DPMM and VDP within the designed chip.

The conventional DVFS technique uses a single power source and adjusts the single supply voltage level, which degrades the circuit power consumption and performance simultaneously. The DPMM is executed by the user first fixing the circuit performance by preplanning the designed circuit in three (performance, low power, and sleep) operation mode. When the user selects a specific mode (e.g. performance), the clock frequency is then fixed. After this, the control signal adapts the appropriate power-switch-control-circuit (PSCC) quantities toward the lowest supply, which also maintain the circuit correct function.

Voltage Domain Programmable (VDP) technique is utilized to support voltage domain programmable (switchable). Power-switch supports the voltage-domain switchable ability. The related detail EDA mechanism to support the VDP planning can be found in [3].

The proposed technique is the circuit design technique to support the performance measurement to support the voltage domain switching functionality. When applying the VDP technique, there are two voltage domains of the designed circuit which require two power sources. The power that supplies high voltage is denoted VddH, and that which supplies low voltage is denoted VddL. Based on the predefined performance requirements, the logic gates' module (M0, M1) voltage can be supplied from VddH or VddL dynamically, dependent on performance-power management criteria. VddH and VddL power source (e.g., 1.5V and 1.2) are used simultaneously. Highly view of the whole designed module can be separated into two groups. One group uses the high-Vdd (VddH) and the other group uses the low-Vdd (VddL). Each designed module can be dynamically changed the belonging group. With this method, we can achieve maximum power savings while obtaining a certain circuit performance. The VddL supply can be also monitored by BIVM as the VDDH.

In Fig. 3, when the BIST (Built-in Self Test) circuitry detects the circuit incorrect function and then does not allow the designed circuit to degrade VddH or increase VCO clock frequency, the voltage-level and clock-frequency adjustment process need to confirm whether the circuit functions are fully correct. A BIST circuit is used to validate the circuit functions. Input test patterns are generated by LFSR (Linear Feedback Shift Register), while the circuit output responses are compressed with self-check by MISR (Multiple Input Shift Register) to identify that the output function is fully correct. The LBO signal is used to indicate the MISR comparison results. The comparison golden outputs need to be pre-stored in advance. Whether BIST mechanism might be executed from input activity function of predefined paths. The golden module's output can be set from critical paths; it is needed to be pre-identified from the designed modules.

In the VDP design performance operation mode, most of the gates consume the current from VddH, while the current from VddL is consumed by few modules. Hence, the VddH voltage level will degrade when the performance mode operation time increases.

The voltage level is detected by the built-in voltage management circuit (BIVM). BIVM captures and measures the voltage level, then transfers it to a digital control signal which decides which operation mode of the circuit to choose. Each circuit module possesses a BIVM to sense the VddH voltage level. The BIVM tracks the VddH voltage level and compares it to the reference voltage (RV) to control the quantities of power switch module (PSM) that are turned on to adjust the VddH level. When the VddH power is above a certain voltage level, the chip operates in performance mode. When the VddH voltage level is degraded, the DPMM mode control circuit switches operation mode to the low power mode, allowing fewer gates to use lower VddH and more gates to use VddL power, which increases the efficiency of utilizing two-type power source. DPMM follows the voltage-level power status, as measured by BIVM, to arrange a suitable voltage domain, which keeps the circuit working in the best performance-power situation.

DPMM proposed on the external power adjusting mechanism. The follows VDP section focus on the designed chip internal mechanism. DPMM and VDP are jointed to manage system's performance-power.

3. The Proposed Module-Level VDP Work

The section illustrates how to reprogram the voltage domain. Figure 4 shows the Dual-Vdd Cluster Voltage Scaling (CVS) technique for a module-level design. In order not to violate the circuit delay time, the logic gates on the critical-path are assigned higher voltage (VddH) while the logic gates on the non-critical paths are assigned lower voltage (VddL) simultaneously. As each designed module can be dynamically changed the group of a designed module belongs to a VddH or VddL. As the voltage-levels are not large different, there are without level shifters adopted between all voltage domains.

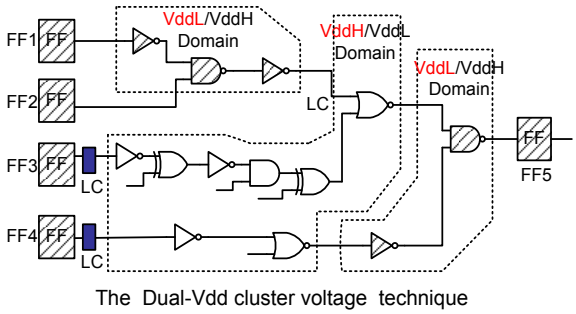


Fig. 4. VDP -multiple voltage domain design methodology.

In the VDP design, the voltage-domain sizes of VddH and VddL are adjustable when a circuit changes to different operational modes. The proposed dual-voltage operated VDP designed circuit is shown in Figure 5. We focus on applying the VDP technique as a module-level design methodology. However, VDP methodology is easier illustrated and demonstrated by a gate-level circuit. When few gates located on the critical paths use VddH, and most gates use VddL, the VDP design consumes less power. In addition, performance-power management modes are adopted VDP for adapting two voltage-level capacities.

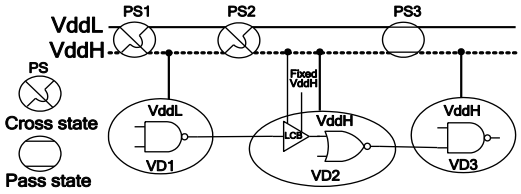
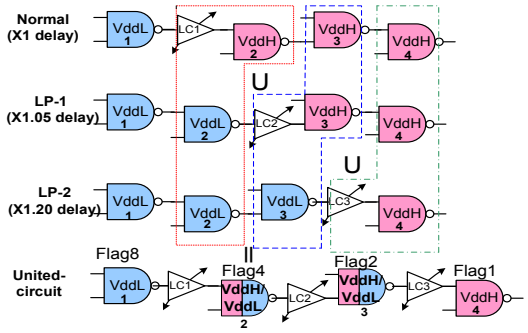


Fig. 5. The voltage domain programmable circuit structure.

By assigning the logic gates with different supply voltages, the circuit delay time vs. power consumption is manageable. LCB means level-converter-buffer, for voltage level adjustment. For example, in the VDP circuit in Figure 6, in the Normal mode, gate_module-1 uses VddL and gates_module-2,3,4 use VddH.

Figure 7 shows in LP-1 mode, gates_module-1,2 use VddL and gates_module -3,4 use VddH. In LP-2 mode, gates_module-1,2,3 use VddL and gate_module-4 uses VddH. Hence, the VddL logic modules are increased when the circuit operates under lower power consumption conditions.

After such assignments, gate_module-1 uses VddL and gate_module-4 uses VddH only, while gates_module-2,3 may use VddH or VddL, depending on the operation mode.



Normal (x1.0)	LP-1 (x1.05)	LP-2 (x1.2)	Flag
VddH	VddH	VddH	1
VddH	VddH	VddL	2
VddH	VddL	VddH	3
VddH	VddL	VddL	4
VddL	VddH	VddH	5
VddL	VddH	VddL	6
VddL	VddL	VddH	7
VddL	VddL	VddL	8

Fig. 6 The voltage domain programmable flag assignment.

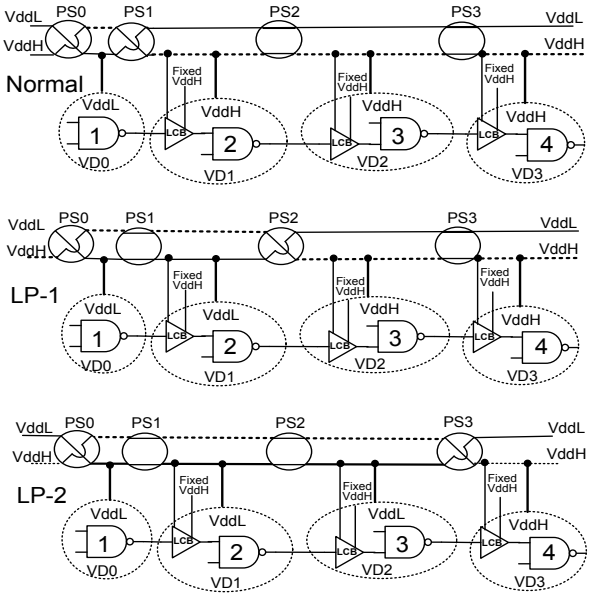


Fig. 7. Power switch state combination for three modes in Fig. 6.

3.1 The Proposed VddH/VddL Switch Circuit

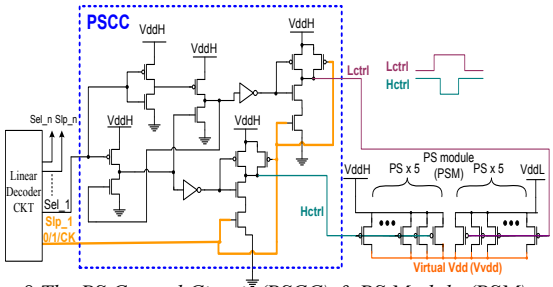


Fig. 8 The PS Control Circuit (PSCC) & PS Module (PSM).

The DPMM provides the VddH and VddL voltages. As there are two voltage sources used, care is needed to prevent the transient current from VddH to VddL during the power switch transfer of the supply voltage. The power switch control circuit (PSCC) will control the PSM circuits so that they do not turn on simultaneously but can quickly switch to the desired voltage domain. PSCC circuit has four operation modes: VddH, VddL, CK_control, and sleep modes. In Figure 8, the voltage adjustment mechanism is processed by power switch quantities, which are turned on in the linear combination. There are a total of 15 PSM-groups attached to the power rings. The 15 PSM groups are controlled by four signals. Each control signal is assigned to turn on 1, 2, 4, or 8 PSM groups simultaneously. The four control signals control the turning on of the PSM with 16 conditions (include sleep mode). A PSM group is built by 10 PSCC circuits. A PSCC circuit includes 10 power switches. This means that there are at most 1500 and at least 100 power switches turned on simultaneously. Then, the VddH voltage level is regulated by the control signals.

4. Chip Design and Measurement Results

Figure 9 shows MPEG VLD Chip die photo and specifications that use TSMC 0.18μm CMOS technology. The chip function proof of this methodology has a significant gain in low power consumption and is successful in power-performance tradeoff applications.

VLD Chip used to validate the feasibility of the proposed VDP technique. Figure 10 shows the power consumption with respect to Single-Vdd and Dual-Vdd. Single-Vdd uses single voltage source (i.e. VddH=VddL=2.2V). Dual-Vdd uses two voltage sources (i.e.

VddH=2.2V, and VddL=1.6V). The power consumption of Dual-Vdd technique is reduced by 55% compared to that of Single-Vdd technique. However, the highest operation frequency in dual-Vdd technique is a little lower than that of single-Vdd technique. However, the paper design lacks comparison to the design systems implemented by DVFS mechanism.

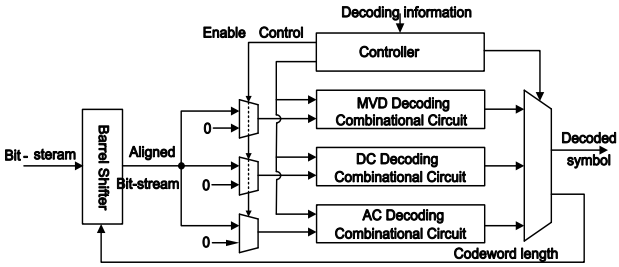
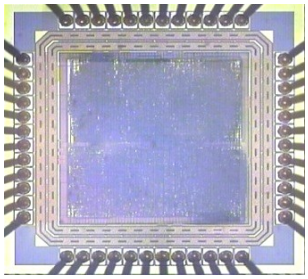


Fig. 9. MPEG VLD Chip-2's architecture constructed by VDP.



Technology	TSMC 0.18um CMOS 1P6M
Supply Voltage	1.6V ~ 2.2V
Chip Size (Inc.PAD)	1.152 x 1.148 mm^2
Core Size	780 x 780 um^2
Gate Count	95138
Operation Frequency	74 MHz (Single-Vdd) 72 MHz (Dual-Vdd)
Power Consumption	39.91 mW (Single-Vdd) 17.59 mW (Dual-Vdd)
Number of pins	48

Fig. 10 VDP designed VLD Chip-2's die photo and specification.

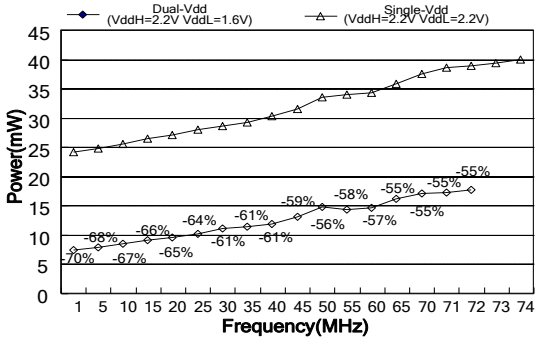


Fig. 11 Power comparison of Chip-2 using Single&Dual-Vdd.

In the performance mode, more modules require higher supply voltage and more current consumption from the VddH. When the chip selects the low power saving mode, current consumption is decreased from few modules using the VddH, but the VddL current consumption is increased.

Higher supply voltages have good performance and large power consumption. Lower supply voltages have large circuit delay time and consume less power. The proposed VDP technique well utilizes the flexibility of the high and low voltages applied to logic modules. The voltage-domain dynamically switchable mechanism supports good performance-power manageable ability.

5. Conclusion

Most of the existing power vs. performance adjustment techniques use the external chip voltage regulating technique. The voltage regulator has a large area and activated-noisy signal when integrated within the designed chip. Most of the current techniques, the regulator is a discrete component in PCB board. The DVFS technique is too complex, and there is no need for the generic design. The main idea in this paper is a coarse-grain dual voltage scheme, in which any designed module can function to select two different supply voltages. This freedom provides good performance-power dynamically managed ability. The contribution of the paper is broad, VDP technique includes circuit design, EDA algorithm. The power integrity issue has taken into design consideration. The proposed mechanism is easily integrated within a system chip, only less area overhead from the requirement of double power mesh networks (10%, estimation). The proposed mechanism allows the chip performance and power consumption to be flexibly adjusted during circuit operation. Two physical implementation chips and measured results proof of this novel methodology has 30~55% power reduction comparisons with using single-Vdd.

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